

#3  
CBurk

<b>TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371</b>		<b>ATTORNEY'S DOCKET NUMBER ROH-037</b>
		<b>U.S. APPLICATION NO. (If known, see 37 C.F.R. 1.5)</b> <b>09/830,092</b>
<b>INTERNATIONAL APPLICATION NO.</b> <b>PCT/JP00/05596</b>	<b>INTERNATIONAL FILING DATE</b> <b>22 August 2000</b>	<b>PRIORITY DATE CLAIMED</b> <b>23 August 1999</b>
<b>TITLE OF INVENTION:</b> <b>SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME</b>		
<b>APPLICANT(S) FOR DO/EO/US</b> <b>Kazutaka SHIBATA</b>		
<p>Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:</p> <ol style="list-style-type: none"> <li>1. <input type="checkbox"/> This is a FIRST submission of items concerning a filing under 35 U.S.C. 371.</li> <li>2. <input checked="" type="checkbox"/> This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371.       <ul style="list-style-type: none"> <li><input type="checkbox"/> This express request to begin national examination procedures (35 U.S.C. 371(f) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(I).</li> <li><input type="checkbox"/> A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.</li> <li><input type="checkbox"/> A copy of the International Application as filed (35 U.S.C. 371(c)(2))           <ul style="list-style-type: none"> <li>a. <input type="checkbox"/> is transmitted herewith (required only if not transmitted by the International Bureau).</li> <li>b. <input type="checkbox"/> has been transmitted by the International Bureau</li> <li>c. <input type="checkbox"/> is not required, as the application was filed in the United States Receiving Office (RO/US).</li> </ul> </li> </ul> </li> <li>6. <input type="checkbox"/> A translation of the International Application into English (35 U.S.C. 371(c)(2)).</li> <li>7. <input type="checkbox"/> Amendment to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).       <ul style="list-style-type: none"> <li>a. <input type="checkbox"/> are transmitted herewith (required only if not transmitted by the International Bureau).</li> <li>b. <input type="checkbox"/> have been transmitted by the International Bureau.</li> <li>c. <input type="checkbox"/> have not been made; however, the time limit for making such amendment has NOT expired.</li> <li>d. <input type="checkbox"/> have not been made and will not be made.</li> </ul> </li> <li>8. <input type="checkbox"/> A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).</li> <li>9. <input checked="" type="checkbox"/> An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).</li> <li>10. <input type="checkbox"/> A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).</li> </ol> <p>Items 11 to 16 below concern either document(s) or information included:</p> <ol style="list-style-type: none"> <li>11. <input type="checkbox"/> In Information Disclosure Statement under 37 CFR 1.97 and 1.98.</li> <li>12. <input checked="" type="checkbox"/> An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.</li> <li>13. <input type="checkbox"/> A FIRST preliminary amendment.       <ul style="list-style-type: none"> <li><input type="checkbox"/> A SECOND or SUBSEQUENT preliminary amendment.</li> </ul> </li> <li>14. <input type="checkbox"/> A substitute specification.</li> <li>15. <input type="checkbox"/> A change of power of attorney and/or address letter.</li> <li>16. <input checked="" type="checkbox"/> Other items or information.</li> </ol> <p>Associate Power of Attorney</p>		

## SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

## BACKGROUND OF THE INVENTION

## Field of the Invention

5       The present invention relates to a method for manufacturing a thin-type semiconductor device. Further, the present invention relates to a semiconductor device having a structure in which a semiconductor chip is bonded onto the surface of a solid device (for example, a wiring 10 substrate or another semiconductor chip), and a method for manufacturing the same.

Further, the present invention relates to a semiconductor device which is advantageous to be three-dimensionally packaged and a method for manufacturing the 15 same.

## Background Art

A back side grinding step for grinding the back side of a semiconductor wafer (hereinafter referred to simply as wafer) in order to thin a semiconductor chip has been 20 conventionally performed. The back side grinding step has been generally performed by adhering a soft protective film onto the surface of a wafer, then urging the wafer against a grinder through the protective film, and rotating the wafer in this state.

25       However, in a cutting out step for cutting individual

semiconductor chips out of the wafer, the wafer is handled by a robot. Further, in a step for mounting each cut-out semiconductor chip on a lead frame, the semiconductor chip is handled by a robot. Therefore, excessive pursuit of  
5 thinning of a semiconductor chip causes the wafer or the semiconductor chip to be broken, so that the yield rate is reduced. Especially nowadays, since wafers become large-diametered, wafers thinned by the back side grinding treatment are apt to be broken.

10 In order to solve these problems, for example, in the Japanese Unexamined Patent Publication (KOKAI) No. 11-150090 (1999), it is proposed that after forming a group of projection electrodes on the surface of a wafer, a resin layer is formed on this surface of the wafer to use the  
15 resin layer as a protective and reinforcing plate.

According to the method of manufacturing a semiconductor device disclosed in this Publication, after forming a resin layer, the back side of a wafer is ground, and further, the surface layer section of the resin layer is removed by etching. Thereby, the projection electrodes are exposed. Thereafter, the resin layer is removed along a scribed line, and further, a nitride layer as a protective layer is formed in the region avoiding the projection electrodes. Then, the wafer is cut along scribed lines to  
20 25 cut out individual semiconductor chips.

According to this method, a wafer, after its back side being ground, is reinforced by a resin layer, and each semiconductor chip is reinforced by the resin layer. And in each semiconductor chip, the projection electrodes 5 functioning as external connection electrodes are embedded in the resin layer. Thereby, the wafer and the semiconductor chip can be satisfactorily handled without being broken, and at the same time, the semiconductor device can be remarkably thinned in comparison with a 10 structure in which outer terminals are pulled out by wire-bonding or the like.

However, it is necessary to perform etching in order to expose the projection electrodes. At the time of etching, etching conditions must be determined so as to surely 15 expose all of the projection electrodes, and therefore, the etching step is complicated and takes much time.

Furthermore, according to the above-mentioned manufacturing method of the prior art, there is a problem that a wafer is warped because of the differences between 20 the thermal expansion/contraction coefficients of the wafer and the resin layer during the time after forming the resin layer on the wafer and before grinding the back side of the wafer. Such a warped wafer is exaggeratedly shown in Fig. 18. When such a warped wafer is ground by 25 a flat grinder, the wafer after being ground has different

thicknesses at the central region and the peripheral region thereof respectively. Consequently, semiconductor chips each having a uniform thickness cannot be obtained and in addition, sometimes a semiconductor chip cut out 5 of the central region of the wafer may not be thinned to a desired thickness.

On the other hand, one of structures capable of heightening the substantial integration density of a semiconductor device is a chip-on-chip structure. In a 10 semiconductor device having a chip-on-chip structure, for example, as shown in Fig. 19, a secondary chip 102 is bonded face-down onto the surface of a primary chip 101, and external connection electrodes 103 are provided on the back side of the primary chip 101. Such a chip-on-chip structure 15 is advantageous to obtain a high integration density of the elements. However, in addition to the thicknesses  $a$ ,  $b$  of the primary chip 101 and the secondary chip 102, the height  $c$  of the external connection electrodes is required. Therefore, it is a defect that the whole height  $(a+b+c)$  20 becomes relatively high.

Further, it is proposed that the space occupied by a semiconductor device is reduced by thinning a semiconductor package and three-dimensionally packaging or mounting the same.

25 Fig. 20 is a sectional view showing an example of a

structure of a semiconductor device 70 proposed for the above-mentioned purpose. In the semiconductor device 70, a thin semiconductor chip 72 is disposed in a punched portion of a tape-shaped substrate 71, and the active 5 surface (the upper surface in Fig. 20) of the semiconductor chip 72 is sealed with a protective resin 73. Inner leads 74 are connected to the semiconductor chip 72 by single point bonding. The connection between the semiconductor chip 72 and an outer packaging substrate 80 is achieved 10 by outer leads 75 connected to the inner leads 74 on the substrate 71. The three-dimensional packaging of the semiconductor device 70 is performed by connecting the outer leads 75 to the packaging substrate 80 respectively.

However, in this structure, it is necessary to 15 individually connect outer leads 75 of each semiconductor device 70 to the packaging substrate 80. Therefore, the three-dimensional packaging steps are complicated and hard to perform.

Further, in this structure, since the outer leads 75 20 are pulled outwardly, there is a problem that the area occupied by the whole of the semiconductor device 70 becomes relatively large.

#### SUMMARY OF THE INVENTION

A first object of the present invention is to provide 25 a method for manufacturing a semiconductor device

capable of surely exposing projection electrodes by a simple step, and therefore capable of simplifying the whole manufacturing steps of the semiconductor device.

A second object of the present invention is to provide  
5 a method for manufacturing a semiconductor device capable of satisfactorily performing a back side grinding treatment of a semiconductor substrate by preventing the semiconductor substrate from being warped, and thereby capable of favorably manufacturing a thin-type  
10 semiconductor device.

A third object of the present invention is to provide a thin-type semiconductor device having a structure in which a semiconductor chip is bonded onto a solid device (for example, chip-on-chip structure), and a method for  
15 manufacturing the same.

A fourth object of the present invention is to provide a semiconductor device which is advantageous to be three-dimensionally packaged or mounted, and a method for manufacturing the same.

20 A method for manufacturing a semiconductor device according to a first aspect of the present invention comprises an electrode forming step of forming projection electrodes on the surface of a semiconductor substrate, a step of forming a protective resin layer on the whole  
25 surface of the semiconductor substrate provided with the

projection electrodes, a back side grinding step of thinning the semiconductor substrate by polishing or grinding the back side of the semiconductor substrate, and a surface grinding step of exposing the projection 5 electrodes by polishing or grinding the surface of the semiconductor substrate.

Either the back side grinding step or the surface grinding step may be performed first.

According to the present invention, the projection 10 electrodes formed on the surface of the semiconductor substrate can be exposed by the surface grinding step comprising polishing or grinding the protective resin layer so formed as to cover the surface of the semiconductor substrate. Therefore, the projection electrodes can be 15 exposed more simply, surely and in a shorter time than by etching. In the back side grinding step and the surface grinding step, the protective resin layer serves to reinforce the semiconductor substrate. Consequently, if the semiconductor substrate is ground to become thin in 20 the back side grinding step, the semiconductor substrate can be handled without hindrance.

In such a manner, a thin-type semiconductor device can be manufactured by a simple manufacturing process and the productivity can be increased.

25 On the semiconductor substrate, a plurality of

elements constituting a plurality of semiconductor devices may be formed. In this case, preferably, a plurality of groups of projection electrodes for the plurality of semiconductor devices are formed in the 5 electrode forming step, and the semiconductor substrate after completing the surface grinding step and the back side grinding step is cut to cut out pieces of semiconductor devices.

According to this method, a plurality of semiconductor 10 devices (semiconductor chips) are formed on a semiconductor substrate (semiconductor wafer). Before cutting out individual semiconductor devices from the substrate, the semiconductor substrate is subjected to the back side grinding treatment and the surface grinding 15 treatment. In this case, the semiconductor substrate before reaching the cutting out step is reinforced by the protective resin layer on its surface. Therefore, if the semiconductor substrate has a small thickness, it is prevented from being broken when handled. Further, in the 20 cutting out step, the semiconductor substrate is protected by the protective resin layer and prevented from being broken.

A method for manufacturing a semiconductor device according to a second aspect of the present invention 25 comprises a step of forming a surface resin layer on the

- surface of a semiconductor substrate, a step of forming  
a back side resin layer on the back side of the  
semiconductor substrate, and a back side grinding step of  
thinning the semiconductor substrate by removing the back  
5 side resin layer, through polishing or grinding, from the  
semiconductor substrate provided with the surface resin  
layer and the back side resin layer, and further polishing  
or grinding the back side of the semiconductor substrate  
from which the back side resin layer has been removed.
- 10        Either the surface resin layer or the back side resin  
layer may be formed first, and the two layers may be formed  
at the same time. However, preferably, the surface resin  
layer and the back side resin layer are formed at such a  
short time interval that a warp of the semiconductor  
15 substrate, if caused, is insignificantly small. Otherwise,  
in order to prevent the semiconductor  
substrate from being significantly warped in the interval  
between forming the surface resin layer and forming the  
back side resin layer, the semiconductor substrate  
20 provided with either one layer is preferably put in a  
temperature-controlled environment till the other layer  
is formed.

According to this invention, since resin layers are  
formed on both of the surface and the back side of the  
25 semiconductor substrate, thermal expansion/contraction

are equally caused in the surface and the back side of the semiconductor substrate. Consequently, in the back side grinding step, the semiconductor substrate is not in an undesirably warped state. Thus, the back side grinding 5 step can be satisfactorily performed, so that the semiconductor substrate can be uniformly thinned in both of the central and peripheral regions. As a result, a thin-type semiconductor device can be favorably manufactured.

10 An embodiment of the present invention further comprises a cutting out step of cutting out individual pieces of semiconductor devices by cutting the semiconductor substrate along cutting lines after completing the back side grinding step.

15 According to this method, a plurality of pieces of semiconductor devices are cut out of the thinned semiconductor substrate. In this case, since the semiconductor substrate is uniformly thinned all over, pieces of thin-type semiconductor devices each having a 20 uniform thickness can be obtained.

The method may further comprise an electrode forming step of forming projection electrodes on the surface of the semiconductor substrate, and a surface grinding step for polishing or grinding the surface resin layer so as 25 to expose the projection electrodes from the surface resin

layer. In this case, either the electrode forming step or the surface grinding step may be performed first. The cutting step is applied to the semiconductor substrate after completing the surface grinding step and the back  
5 side grinding step.

A semiconductor device of a first aspect of the present invention comprises a first semiconductor chip (an example of a solid device), a second semiconductor chip bonded onto the surface of the first semiconductor chip, projection  
10 electrodes for external connection formed on the surface of the first semiconductor chip, and a protective resin for sealing the surface of the first semiconductor chip in the state in which the head portions of the projection electrodes are exposed therefrom.

15 In this structure, the second semiconductor chip is bonded onto the surface of the first semiconductor chip. And the projection electrodes are formed on the same surface of the first semiconductor chip, and the surface of the first semiconductor chip is sealed with the protective resin in the state in which the head portions  
20 of the projection electrodes are exposed. Consequently, the whole height of the semiconductor device can be reduced in comparison with a case in which external connection electrodes are provided on the back side of the first  
25 semiconductor chip. As a result, a thin-type chip-on-chip

semiconductor device can be realized.

The head portions of the projection electrodes may be in the same plane with the protective resin or may be protruded from the surface of the protective resin.

5 Further, as long as the head portions of the projection electrodes are exposed, the head portions of the projection electrodes may be depressed inwardly from the surface of the protective resin.

Further, the second semiconductor chip may be embedded  
10 in the protective resin, or an inactive surface or a part  
of each side surface of the second semiconductor chip may  
be exposed from the protective resin.

A chip-on-chip type semiconductor device having the above-mentioned structure can be manufactured by a method  
15 comprising a chip bonding step of bonding a plurality of semiconductor chips face-down e.g. onto the surface of a semiconductor substrate with their active surfaces opposed to the surface of the semiconductor substrate, an electrode forming step of forming a plurality of  
20 projection electrodes on the surface of the semiconductor substrate, a resin sealing step of sealing, with a protective resin, the semiconductor chip and the exposed surface of the semiconductor substrate after forming the projection electrodes in such a manner that the head  
25 portions of the projection electrodes are exposed, and a

cutting out step for taking out pieces of chip-on-chip type semiconductor devices by cutting the semiconductor substrate along the predetermined cutting lines.

According to this method, a plurality of semiconductor  
5 chips are bonded onto the surface of the semiconductor substrate, and at the same time, a plurality of projection electrodes are formed on the same surface of the semiconductor substrate. Therefore, in the state of a semiconductor substrate (semiconductor wafer), bonding of  
10 the semiconductor chips and forming of the projection electrodes can be performed. And thereafter, by cutting pieces of chip-on-chip type semiconductor devices out of the semiconductor substrate, a plurality of chip-on-chip type semiconductor devices can be efficiently  
15 manufactured.

Since the surface of the semiconductor substrate is sealed with the protective resin and the semiconductor chips are bonded face-down onto the surface of the semiconductor substrate, the surface of the semiconductor  
20 substrate and each surface (active surface) of the semiconductor chip are sufficiently protected. Consequently, it is possible to realize a thin-type semiconductor package having a height nearly equal to the sum of the thicknesses of the semiconductor substrate and  
25 the semiconductor chip mounted thereon.

Further, by polishing or grinding the back side of the semiconductor substrate and the back surface side (inactive surface side) of the semiconductor chip by a grinder or the like, before a cutting out step, at need,  
5 a thinner semiconductor device can be obtained.

The above-mentioned resin sealing step preferably includes an electrode exposing step of exposing the head portions of the projection electrodes by removing the surface layer section of the protective resin. Thereby,  
10 the projection electrodes can be surely exposed.

The surface layer section of the protective resin may be removed by grinding using a grinder or the like, but another method such as etching may be applied.

The above-mentioned electrode exposing step  
15 preferably includes a chip grinding step of simultaneously polishing or grinding the protective resin and the inactive surface side of the semiconductor chip. Thereby, the projection electrodes can be surely exposed and at the same time the semiconductor chip can be thinned.

20 A semiconductor device according to the second aspect of the present invention comprises a substrate (an example of a solid device), a semiconductor chip bonded face-down onto the surface of the substrate with its active surface opposed to the surface of the substrate, projection  
25 electrodes formed on and protruded from the surface of the

substrate onto which the semiconductor chip is bonded, and a protective resin for sealing the projection electrodes and the semiconductor chip in such a manner that the head portions of the projection electrodes are exposed.

5       The projection electrodes are preferably provided surrounding the semiconductor chip (as close as possible to the semiconductor chip).

Further, the above-mentioned substrate is preferably a thin-type substrate such as a tape-shaped substrate or  
10      the like.

According to this invention, a semiconductor chip and projection electrodes functioning as external connection electrodes are provided on the surface on the same side of a substrate. In this structure, by forming through holes  
15      in the substrate for enabling the electrical connection from the back side of the substrate to the base portions of the projection electrodes, a plurality of three-dimensionally stacked semiconductor devices can be easily electrically connected to one another through the  
20      through holes.

Besides, by using projection electrodes, the area occupied by a semiconductor device can be reduced, and the lengths of the wirings of connecting three-dimensionally packaged or mounted semiconductor devices to one another  
25      can be shortened.

The above-mentioned through holes are preferably formed at the positions right below the projection electrodes.

The above-mentioned semiconductor device can be  
5 manufactured by a method comprising a chip bonding step  
of bonding a semiconductor chip face-down on the surface  
of a substrate with its active surface opposed to the  
surface of the substrate, an electrode forming step of  
forming a plurality of projection electrodes on the  
10 surface of the substrate so as to be protruded from the  
surface of the substrate, and a resin sealing step of  
sealing, with a protective resin, the semiconductor chip  
and the projection electrodes in such a manner that the  
head portions of the projection electrodes are exposed.  
15

According to an embodiment of this method, a plurality  
of semiconductor chips are bonded onto the substrate in  
the chip bonding step, and a plurality of groups of  
projection electrodes corresponding to the plurality of  
semiconductor chips are formed in the electrode forming  
20 step. And by cutting the substrate along the predetermined  
cutting lines, pieces of semiconductor devices are cut  
out.

By this method, a plurality of semiconductor devices  
can be manufactured at the same time.

25 In this case, the resin sealing step is preferably

performed so as to seal the plurality of semiconductor chips and the plurality of projection electrodes as a whole. The protective resin for sealing the plurality of semiconductor chips may be integrated or separated for 5 each semiconductor chip. When the protective resin for sealing the plurality of semiconductor chips is integrated, preferably the protective resin and the substrate are cut at the same time in the cutting out step. Therefore, it is preferable to perform the cutting out step after the 10 resin sealing step.

The resin sealing step may include a step of sealing, with a protective resin, the projection electrodes and the semiconductor chips, and a step of removing the surface layer section of the protective resin so as to expose the 15 head portions of the projection electrodes.

Preferably, the above-mentioned method for manufacturing a semiconductor device may further comprise a step of thinning the semiconductor chip by polishing or grinding the inactive surface of the semiconductor chip. 20 In this step, the whole of the device may be thinned by polishing or grinding the protective resin at the same time.

Preferably, for performing three-dimensional packaging or mounting, the method further comprises a step 25 of forming through holes in the substrate for enabling the

electrical connection from the back side of the substrate to the base portions of the projection electrodes. In this case, the through holes are preferably formed at the positions right below the projection electrodes.

5       The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of embodiments of the present invention given with the accompanying drawings.

10      BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1(a) to 1(e) are schematically sectional views showing steps in order of a method for manufacturing a semiconductor device according to a first embodiment of the present invention.

15      Fig. 2 is a schematically perspective view of a semiconductor device manufactured by the method of Figs. 1(a) to 1(b).

Figs. 3(a) to 3(f) are schematically sectional views showing steps in order of a method for manufacturing a 20 semiconductor device according to a second embodiment of the present invention.

Fig. 4 is a schematically perspective view of a semiconductor device manufactured by the method of Figs. 3(a) to 3(e).

25      Fig. 5 is a perspective view showing the structure of

a semiconductor device according to a third embodiment of the present invention.

Figs. 6(a) to 6(e) are sectional views showing steps in order of a method for manufacturing the semiconductor 5 device of Fig.5.

Fig. 7 is a sectional view showing the structure of a semiconductor device according to another embodiment of the present invention.

Fig. 8 is a sectional view showing the structure of 10 a semiconductor device according to a further embodiment of the present invention.

Fig. 9 is a sectional view explaining steps of a method for manufacturing a semiconductor device according to a further embodiment of the present invention.

15 Fig. 10 is a perspective view showing the structure of a semiconductor device according to an embodiment of the present invention.

Figs. 11(a) to 11(f) are sectional views showing steps in order of a method for manufacturing the semiconductor 20 device of Fig.10.

Fig. 12 is an enlarged sectional view showing the structure in the vicinity of the projection electrodes.

Fig. 13 is a perspective view explaining the three-dimensional packaging of the abovementioned 25 semiconductor devices.

Fig. 14 is a perspective view showing the structure for connecting specified projection electrodes of a specified semiconductor device to a packaging substrate independently of other semiconductor devices.

5 Fig. 15 is a sectional view showing three-dimensional packaging of semiconductor devices containing different-sized semiconductor chips.

Fig. 16 is a sectional view showing the structure of 10 a semiconductor device according to an eighth embodiment of the present invention.

Fig. 17 is a sectional view showing the structure of a semiconductor device according to a ninth embodiment of the present invention.

15 Fig. 18 is a schematic view explaining a problem of warping caused when a resin layer is formed only on the surface of a wafer.

Fig. 19 is a schematic view explaining the structure of a conventional chip-on-chip type semiconductor device.

20 Fig. 20 is a sectional view showing an example of a three-dimensional packaging of a thin-type semiconductor device by a prior art.

#### MODES FOR CARRYING OUT THE INVENTION

Figs. 1(a) to 1(e) are schematically sectional views showing steps in order of a method for manufacturing a 25 semiconductor device according to an embodiment of the

present invention. A semiconductor wafer W (hereinafter referred to simply as wafer W) has been subjected to a variety of element forming steps, wiring forming steps and the like, and its surface 1 on an active surface layer 5 region side is covered with a protective layer (passivation layer) comprising a nitride layer or the like. A pad (not shown) for external electric connection is exposed from the protective layer.

As shown in Fig. 1(a), a plurality of projection 10 electrodes T made of, for example, gold (Au) are formed on the pad (electrode forming step). Preferably, these projection electrodes T are formed by, for example, electrolytic plating, and the height of each projection electrode T from the surface of the protective layer is, 15 for example, about 25  $\mu$ m. Each projection electrode T is in the form of a cylinder such as a circular cylinder or a rectangular cylinder. In addition to gold, solder and the like can be used as the material of the projection electrodes.

After forming the projection electrodes T, as shown 20 in Fig. 1(b), a protective resin layer 3 is formed over substantially the whole of the surface of the wafer W (protective resin layer forming step). The protective resin layer 3 is formed of, for example, an epoxy resin 25 or the like and by, for example, a screen printing method.

Preferably, the protective resin layer 3 has a thickness capable of embedding the projection electrodes T thereinto. In concrete, the protective resin layer 3 preferably has a thickness of about  $100 \mu\text{m}$  and such a protective resin layer 3 can fulfill its function of reinforcing the wafer W which has been subjected to the back side grinding treatment even after the following surface grinding treatment.

Thereafter, as shown in Fig. 1 (c), the back side 2 of the wafer W is ground, for example, using a grinder (back side grinding step). Thereby the wafer W is thinned to a predetermined thickness  $t_w$  (for example,  $t_w$  being about  $50 \mu\text{m}$ ). Since the surface 1 of the wafer W is protected by the protective resin layer 3, it is not necessary to use a protective film or the like for protecting the wafer W in the back side grinding step.

Further, as shown in Fig. 1 (d), the surface 1 of the wafer W is ground similarly using, for example, a grinder (surface grinding step). Precisely, the surface of the protective resin layer 3 is ground to expose the head portions of the projection electrodes T, and after the projection electrodes T are exposed, both of the protective resin layer 3 and the projection electrodes T are simultaneously ground. This surface grinding treatment is performed till the thickness  $t_3$  of the

protective resin layer 3 becomes, for example, about 50  $\mu\text{m}$ . After the surface grinding step is completed, the surface of the protective resin layer 3 and the top surfaces of the projection electrodes T are in the same plane. In 5 this surface grinding step, the back side of the wafer W must be held by, for example, a vacuum chuck device, but it need not be particularly protected by a protective film or the like.

Thereafter, as shown in Fig. 1(e), the protective 10 resin layer 3 and the wafer W are cut by a dicing saw 5 along scribed lines, and pieces of semiconductor chips C, the perspective view of each of which is shown in Fig. 2, are cut out (cutting out step).

In the back side grinding step and the surface 15 grinding step, the whole of the wafer w is reinforced by the protective resin layer 3 formed on the surface 1 of the wafer W. Therefore, the wafer W is satisfactorily ground without being broken, so that thinning of the wafer W can be advantageously performed.

Further, in handling the wafer W before the cutting 20 out step and in cutting the wafer W by the dicing saw 5, the protective resin layer 3 reinforces the wafer W, and therefore, the wafer W and the semiconductor chips C are prevented from being broken. Accordingly, the wafer W can 25 be thinned to a desired thickness, which can contribute

to thinning of the semiconductor chips.

In the final shape of the semiconductor chip C shown in Fig. 2, the protective resin layer 3 protects the surface 1 (active surface) of the wafer W. Further, the top 5 surfaces of the projection electrodes T are exposed from the protective resin layer 3. Therefore, it is not necessary to package additionally the semiconductor chip C. By the abovementioned steps, highly thinned semiconductor package can be obtained.

According to this embodiment, as abovementioned, it is possible to manufacture thin-type semiconductor chips C in which the projection electrodes T are surely exposed, by simple and short time treatment of grinding a wafer W from both sides of the surface and the back thereof. This 15 can simplify the process of manufacturing thin-type semiconductor chips C and contribute to the improvement of the productivity thereof.

In the abovementioned embodiment, the back side grinding step (Fig. 1 (c)) is performed first, and then 20 the surface grinding step (Fig. 1(d)) is performed. However, it is possible to perform the surface grinding step first and then the back side grinding step.

Figs. 3(a) to 3(f) are schematically sectional views showing steps in order of a method for manufacturing a 25 semiconductor device according to a second embodiment of

the present invention. In Figs. 3(a) to 3(f), parts corresponding to the parts in Figs. 1(a) to 1(e) are given the same reference characters with those of the parts in Figs. 1(a) to 1(e).

5 A semiconductor wafer W (hereinafter referred to simply as wafer W) shown in Figs. 3(a) to 3(e) has been subjected to a variety of element forming steps, wiring forming steps and the like, and its surface 1 on an active surface layer region side is covered with a protective layer (passivation layer) comprising a nitride layer. A pad (not shown) for external electric connection is exposed from the protective layer.

10 As shown in Fig. 3(a), a plurality of projection electrodes T made of, for example, gold (Au) are formed on the pad (electrode forming step). Preferably, these projection electrodes T are formed by, for example, electrolytic plating, and the height of each projection electrode T from the protective layer is, for example, about 50  $\mu$ m. Each projection electrode T is in the form 15 of a cylinder such as a circular cylinder or a rectangular cylinder. In addition to gold, solder and the like can be used as the material of the projection electrodes.

20 After forming the projection electrodes T, as shown in Fig. 3(b), a protective resin layer is formed over substantially the whole of the surface of the wafer W

(protective resin layer forming step). The protective resin layer 3 is formed of, for example, an epoxy resin or the like and by, for example, a screen printing method. Preferably, the protective resin layer 3 has a thickness 5 capable of embedding the projection electrodes T thereinto.

In concrete, the protective resin layer 3 preferably has a thickness of about 100  $\mu\text{m}$  and such a protective resin layer 3 can fulfill its function of reinforcing the wafer W which has been subjected to the back side grinding 10 treatment even after the following surface grinding treatment.

After forming the protective resin layer 3, a back side resin layer 4 is formed over substantially the whole of the back side 2 of the wafer W as shown in Fig. 3(c). 15 Preferably, the back side resin layer 4 is formed of the same material as that of the protective resin layer 3 and has a thickness substantially equal to that of the protective resin layer 3. Further, the back side resin layer 4 can be formed by a similar forming method to that 20 of the protective resin layer 3.

Preferably, the protective resin layer 3 forming step and the back side resin layer 4 forming step are performed successively or simultaneously in order to prevent such a temperature change as causing warping of the wafer W. 25 If it is necessary to form the back side resin layer 4 a

relatively long time after forming the protective resin layer 3, the wafer W after completing the protective resin layer 3 forming step is preferably put in a temperature-controlled environment in order to prevent 5 warping of the wafer W caused by the differences between the thermal expansion/contraction coefficients of the protective resin layer 3 and the wafer W.

After the back side resin layer 4 is formed on the back side 2 of the wafer W, as shown in Fig.3(d), the surface 10 1 of the wafer W is ground using, for example, a grinder (surface grinding step). Precisely, the surface of the protective resin layer 3 is ground to expose the head portions of the projection electrodes T, and after the projection electrodes T are exposed, both of the 15 protective resin layer 3 and the projection electrodes T are simultaneously ground. This surface grinding is performed till the thickness  $t_3$  of the protective resin layer 3 becomes, for example, about  $40 \mu m$ . After the surface grinding step is completed, the surface of the 20 protective resin layer 3 and the top surfaces of the projection electrodes T are in the same plane. In this back side grinding step, the back side of the wafer W must be held by, for example, a vacuum chuck device, and at that time the back side 2 of the wafer W is protected by the 25 back side resin layer 4.

Further, as shown in Fig. 3(e), the back side grinding step is performed, similarly, for example, using a grinder. In other words, the back side resin layer 4 is ground and removed away, and further the back side 2 of the wafer W 5 is successively ground. Thereby the wafer W is thinned to a predetermined thickness  $t_w$  (for example,  $t_w$  being about 100  $\mu\text{m}$ ). Since the surface 1 of the wafer W is protected by the protective resin layer 3, it is not necessary to use a protective film or the like for protecting the wafer 10 W in the back side grinding step.

Thereafter, as shown in Fig. 3(f), the protective resin layer 3 and the wafer W are cut by a dicing saw 5 along scribed lines (cutting lines) and pieces of semiconductor chips C, the perspective view of each of 15 which is shown in Fig. 4, are cut out (cutting out step).

In the back side grinding step and the surface grinding step, the whole of the wafer w is reinforced by the protective resin layer 3 formed on the surface 1 of the wafer W. Therefore, the wafer W is satisfactorily 20 ground without being broken, so that thinning of the wafer W can be advantageously performed.

Further, in handling the wafer W before the cutting out step and in cutting the wafer W by the dicing saw 5, the protective resin layer 3 reinforces the wafer W, and 25 therefore, the wafer W and the semiconductor chips C are

prevented from being broken. Accordingly, the wafer W can be thinned to a desired thickness, which can contribute to thinning of the semiconductor chips.

In the final shape of the semiconductor chip C shown  
5 in Fig. 4, the protective resin layer 3 protects the surface  
1 (active surface) of the wafer W. Further, the top  
surfaces of the projection electrodes T are exposed from  
the protective resin layer 3. Therefore, it is not  
necessary to package additionally the semiconductor chip  
10 C. By the above-mentioned steps, highly thinned  
semiconductor packages can be obtained.

As mentioned above, in this embodiment, a protective resin layer 3 is formed on the surface 1 of a wafer W and a back side resin layer 4 is formed on the back side 2 of  
15 the wafer W, so that thermal expansion/contraction on the surface and the back side of the wafer W equally occur. Therefore, in the surface grinding step (Fig. 3(d)) and the back side grinding step (Fig. 3(e)), warp of the wafer W does not occur. Accordingly, each of the protective resin  
20 layer 3 and the back side 2 of the wafer W can be ground uniformly in any portion of the wafer W. As a result, a plurality of chips C cut out by the cutting out step (Fig. 3(f)) have a uniform thickness.

When a wafer W is, for example, in the state  
25 immediately after completing the surface grinding step as

shown in Fig. 3 (d)), the resin layers 3, 4 on the surface and the back side of the wafer W respectively are different in thickness from each other. And if the warp of the wafer W caused by the difference in thickness between the layers 5 3, 4 becomes a problem, it can be solved by holding the surface and the back side of the wafer by, for example, a chuck. After the back side grinding step is completed, the protective resin layer 3 is sufficiently thinned, so that undesirable warp of the wafer W can be prevented from 10 occurring.

Though the surface grinding step (Fig. 3(d)) is performed first and then the back side grinding step (Fig. 3(e)) is performed in the above-mentioned embodiment, the surface grinding step may be performed after the back side 15 grinding step. However, for the purpose of grinding a protective resin layer 3 uniformly in any portion of the wafer W, it is preferable to perform the surface grinding step first.

Fig.5 is a perspective view showing the structure of 20 a semiconductor device according to a third embodiment of the present invention. The semiconductor device 10 has a chip-on-chip structure in which a secondary chip D (the second chip) is bonded face-down onto the surface (active surface) of a primary chip M(the first chip) with the 25 surfaces (active surfaces) of the two chips M,D opposed

to each other. Each of the primary chip M and the secondary chip D is formed of, for example, a silicon chip, and active elements such as a transistor, passive elements such as a resistance and a capacitor, wiring or the like are formed  
5 on the surface of each chip.

In this embodiment, each of the primary chip M and the secondary chip D is formed in a rectangular shape when viewed in plan, and the secondary chip D is somewhat smaller than the primary chip M when viewed in plan. A plurality  
10 of projection electrodes (cylindrical electrodes in this embodiment) T functioning as external connection electrodes are provided in a region surrounding the secondary chip D on the surface (active surface) of the primary chip M.

15 The region, in which the secondary chip D or the projection electrodes T are not provided, of the surface of the primary chip M is sealed with a protective resin (for example, epoxy resin) 11 so as to protect the surface of the primary chip M. Since the surface of the secondary  
20 chip D is opposed to the primary chip M and the side surfaces of the secondary chip D are sealed with the protective resin 11, the secondary chip D is protected from outside.

In this embodiment, the protective resin 11, the top surfaces of the projection electrodes T and the inactive  
25 surface of the secondary chip D are in the same plane.

The semiconductor device 10 with such a structure can be formed to be an extremely thin semiconductor device having a height nearly equal to the sum of the thicknesses of the primary chip M and the secondary chip D. Therefore,  
5 a thin-type chip-on-chip semiconductor device can be realized.

Figs. 6(a) to 6(e) are sectional views showing steps in order of a method for manufacturing the above-mentioned semiconductor device 10. A protective layer (passivation layer) comprising a nitride layer or the like is formed on the surface (active surface) Wa of a semiconductor wafer W (hereinafter referred to simply as wafer W) as a semiconductor substrate. And pads of internal wiring are exposed from a plurality of portions of the protective  
10 layer in which external connections are required. As shown in Fig. 6 (a), a plurality of projection electrodes T and a plurality of bumps B are formed on these pads (electrode forming step). The projection electrodes T are formed on the pads for external connection, while the bumps B are formed on the pads for chip-to-chip connection to be connected to the secondary chip D. The projection electrodes T and the bumps B can be formed of the same material, and they are preferably formed of an  
15 oxidization-resisting metal, for example, gold. Further,  
20 the projection electrodes T are preferably formed to be  
25

higher than the bumps B.

Thereafter, as shown in Fig. 6(b), the secondary chip D is bonded face-down onto the surface Wa of the wafer W with the surface (active surface) Da of the secondary chip D opposed to the surface Wa of the wafer W (chip bonding step). And then, the surface Wa of the wafer W, the projection electrodes T and the bumps B are resin-sealed with a protective resin 11 (resin sealing step). At this time, the head portions of the projection electrodes T and/or the back side (inactive surface) Db of the secondary chip D may be left exposed from the protective resin 11, as long as the exposed portions of the surface Wa of the wafer W are covered with the protective resin 11.

Then, as shown in Fig. 6(c), the back side (inactive surface) Wb of the wafer W is polished or ground by a grinder, thereby further thinning the semiconductor device.

Thereafter, as shown in Fig. 6(d), the projection electrodes T are exposed by polishing or grinding the protective resin 11 by a grinder (electrode exposing step). Further, after the grinding position reaches the inactive surface Db of the secondary chip D, the protective resin 11 and the inactive surface Db of the secondary chip D are simultaneously polished or ground (chip grinding step), thereby further thinning the secondary chip D and the protective resin 11.

After that, as shown in Fig. 6(e), the wafer W and the protective resin 11 are cut along scribed lines (cutting lines) L by a dicing saw 15. As a result, pieces of semiconductor devices 10 having a structure shown in Fig. 5 are cut out, in each of which a secondary chip D is bonded onto a primary chip M cut out of the wafer W.

Either of the step of Fig. 6(c) and the step of Fig 6(d) may be performed first, and the step of Fig. 6(c) may be omitted if unnecessary.

According to this embodiment, as mentioned above, a secondary chip D is bonded onto a primary chip M before the primary chip M is cut out of a wafer W, and projection electrodes T functioning as external connection electrodes are formed on the surface Wa of the wafer W on which the secondary chip D is bonded. Further, by cutting the wafer W with its surface Wa protected by a protective resin 11, pieces of packaged semiconductor devices 10 having a chip-on-chip structure can be obtained. Therefore, it is possible to efficiently manufacture thin-type chip-on-chip semiconductor devices.

In the above-mentioned embodiment, the protective resin 11, the projection electrodes T and the inactive surface Db of the secondary chip D are in the same plane. However, the head portions of the projection electrodes 25 T may be protruded from the surface of the protective resin

11 as in the fourth embodiment shown in Fig. 7. Further,  
the inactive surface Db side of the secondary chip D may  
be protruded from the protective resin 11 as in the fifth  
embodiment shown in Fig. 8. The structures shown Figs. 7  
5 and 8 can be formed, for example, by sufficiently thinning  
the protective resin 11. In these cases, if the protective  
resin 11 tends to adhere to the head portions of the  
projection electrodes T, the protective resin adhered to  
the head portions of the projection electrodes T can be  
10 removed by polishing or grinding by a grinder or etching.

Further, in the above-mentioned embodiment, the  
projection electrodes T are higher than the inactive  
surface Db of the secondary chip D. However, the height  
of the projection electrodes T may be lower than the  
15 inactive surface Db of the secondary chip D, as in the sixth  
embodiment shown in Fig. 9 (the height being, for example,  
less than  $100 \mu m$ ). Even in this case, after the back side  
grinding step (grinding to the position indicated by a  
solid line) and the surface grinding step (grinding to the  
20 position indicated by a two dots and dash line) are  
completed, the same structure as that of the first  
embodiment can be obtained. By making low the height of  
the projection electrodes T, the projection electrodes T  
can be easily formed in a short time and the material  
25 thereof can be reduced. Thereby the productivity can be

improved and the manufacturing cost can be reduced. However, in order to grind simultaneously the secondary chip D and the projection electrodes T and thereby make their surfaces in the same plain, the height of each 5 projection electrode T formed at the beginning is preferably higher than the active surface Da of the secondary chip D.

Further, in the above-mentioned embodiment, an example is described in which a secondary chip D is bonded 10 to a primary chip M. However, two or more secondary chips D may be bonded to a primary chip M.

Further, though each of the projection electrodes T is in the form of a cylinder in the above-mentioned embodiment, it may be in the form of a bump.

15 Furthermore, in the abovementioned embodiment, the primary chip M and the secondary chip D are formed of silicon semiconductors, respectively. However, in addition to silicon semiconductors, semiconductor chips formed of other arbitrary materials such as gallium 20 arsenic semiconductors or germanium semiconductors can be applied to a semiconductor device according to the present invention. In this case, the semiconductor materials of the primary chip M and the secondary chip D may be the same or different from each other.

25 Fig. 10 is a perspective view showing the structure

of a semiconductor device according to the seventh embodiment of the present invention. The semiconductor device 20 has a structure in which a semiconductor chip C is bonded face-down onto the surface of a tape-shaped 5 wiring substrate 21 such as a polyimide substrate or a glass epoxy substrate with the active surface of the semiconductor chip C opposed to the surface of the substrate 21. In this embodiment, the semiconductor chip C is formed in a rectangular shape when viewed in plan.

10 A plurality of projection electrodes (cylindrical electrodes in this embodiment) T protruded from the surface of the substrate 21 and functioning as external connection electrodes are provided in a region surrounding the semiconductor chip C.

15 The region, in which the semiconductor chip C or the projection electrodes T are not provided, of the surface of the substrate 21 is resin-sealed with a protective resin (for example, epoxy resin) 25. The protective resin 25 reinforces the whole of the semiconductor device 20 and 20 serves to prevent the projection electrodes T from being deformed. Since the surface of the semiconductor chip C is opposed to the substrate 21 and the side surfaces of the semiconductor chip C are sealed with the protective resin 25, the semiconductor chip C is protected from 25 outside.

In this embodiment, the protective resin 25, the head surfaces of the projection electrodes T and the inactive surface C<sub>b</sub> of the semiconductor chip C are in the same plane.

- 5       Figs. 11(a) to 11(e) are sectional views showing steps in order of fabricating the above-mentioned semiconductor device. Fig. 11(a) shows a semiconductor chip bonding step. A wiring pattern is preliminarily formed on the substrate 21 such as a polyimide substrate, for example, by copper electrolytic plating or the like. On the wiring pattern, 10 a plurality of projection electrodes T are formed (electrode forming step). A plurality of semiconductor chips C are bonded face-down onto the surface 21a of the substrate 21 on which the projection electrodes T are formed. That is, each of the semiconductor chips C is bonded, 15 through bumps B formed thereon, onto the substrate 21 with its active surface C<sub>a</sub> i.e. the surface on the active surface layer side on which elements such as a transistor and a resistance are formed being opposed to the substrate 21, and the semiconductor chips C are electrically connected 20 to the wiring pattern formed on the substrate 21. As a result, the semiconductor chips C are electrically connected to the projection electrodes T through the wiring pattern formed on the substrate 21.
- 25       The semiconductor chips C bonded onto the substrate

21 have a rather large thickness, for example, about 300  $\mu\text{m}$  to 700  $\mu\text{m}$ . Such semiconductor chips C can be obtained by dividing a 300  $\mu\text{m}$  to 700  $\mu\text{m}$  thick semiconductor wafer (not shown) by a dicing saw. Such a sufficiently thick wafer  
5 are not broken or chipped off in the dicing step. In addition, the thick semiconductor chips C obtained through the dicing step are not broken or chipped off in the subsequent handling process for bonding the same onto the substrate 21.

10 After the semiconductor chips C are bonded onto the substrate 21, a liquid resin (underfill) is injected into spaces between the active surfaces Ca and the substrate 21 at need.

Fig. 11(b) shows a resin sealing step performed  
15 subsequently to the semiconductor chip bonding step. In this resin sealing step, a metal mold (not shown) is used. Formed in this metal mold is a cavity for wholly containing the semiconductor chips C bonded onto the substrate 21 and the projection electrodes T provided around the  
20 semiconductor chips C. And the semiconductor chips C on the substrate 21 and the projection electrodes T are wholly sealed with the protective resin 25 (resin sealing step). Thereby, the side walls 32 and the inactive surface Cb in opposite to the active surface Ca of each semiconductor  
25 chip C are covered with the protective resin 25, and each

projection electrode T is wholly embedded in the protective resin 25. Further, the side portions of the space between each active surface Ca and the substrate 21 are sealed with the protective resin 25, so that the active 5 surface Ca is protected.

However, in this resin sealing step, the head portion of each projection electrode T and/or the back side (inert surface) Cb of each semiconductor chip C may be left exposed from the protective resin 25.

10 Fig. 11(c) shows a grinding step performed subsequently to the resin sealing step and after the protective resin 25 is hardened. In this grinding step, grinding is carried out to a grinding target thickness To using a grinder. That is, the protective resin 25 is ground 15 and thereby the inactive surfaces Cb of semiconductor chips C are exposed. After that, grinding of the protective resin 25 and grinding of the inactive surface Cb side of the semiconductor chips C are simultaneously carried out, to reach the grinding target thickness To. The grinding 20 target thickness To is set so that the thickness t of the semiconductor chip C after being ground becomes, for example, about 100  $\mu\text{m}$  to 200  $\mu\text{m}$ .

Then, as shown in Fig. 11(d), the protective resin 25 and the substrate 21 are cut along cutting lines D provided 25 between semiconductor chips C e.g. using a dicing saw 35,

thereby pieces of semiconductor devices 20 being cut out as shown in Fig. 11(e). In each semiconductor device 20 cut out by this cutting out step, the whole of the side walls of the semiconductor chip C are covered with the 5 protective resin 25. The upper surface 25a of the protective resin 25 and the inactive surface Cb after being ground are in the same plane, and the corners of the semiconductor chip C is covered with the protective resin 25, so that the semiconductor chip C is protected in any 10 portion thereof.

In each piece of semiconductor device 20 thus cut out, as shown in Fig. 11(e), through holes 27 are provided at need in the substrate 21 at the positions right below the base portions of the projection electrodes T. These 15 through holes 27 are provided so that electric connection can be made from the back side of the substrate 21 to the projection electrodes T through the through holes 27.

Further, as shown in Fig. 11(f), e.g. solder balls 28 are formed at need in the through holes 27 by being 20 transferred by printing. The solder ball 28 is connected at need to the wiring pattern 33 formed on the surface 21a side of the substrate 21 through the through hole 27 by reflowing, as shown in Fig. 12. The semiconductor chip C is connected through a bump B to this wiring pattern 33, 25 and the projection electrode T is bonded to the wiring

pattern 33 at another position.

Fig. 13 is a perspective view explaining three-dimensional packaging or mounting of the above-mentioned semiconductor devices 20. On the surface 5 of the packaging or mounting substrate 50, a print wiring 51 is formed of copper or the like and a packaging region 52 of the semiconductor devices 20 is set. On the packaging region 52, a plurality of semiconductor devices 20 are stacked and packaged. The plurality of semiconductor 10 devices 20 may contain the same or different kinds of semiconductor chips C, respectively.

The layers of semiconductor devices 20 are electrically connected to one another by connecting the projection electrodes T of the layers of semiconductor 15 devices 20 to one another through the through holes 27 in the substrates 21 thereof (refer to Figs. 11(a) to 11(e) and Fig. 12). And the layers of semiconductor devices 20 are electrically connected to a circuit on the packaging substrate 50 by connecting the projection electrodes T of 20 the lowest layer (the closest layer to the packaging substrate 50) of semiconductor device 20 to the print wiring 51 on the packaging substrate 50 through the through holes 27. The connection of the layers of semiconductor devices 20 to one another and the connection of the lowest 25 layer of semiconductor device 20 to the print wiring 51

are achieved by melting the solder balls 28 through reflowing.

According to this embodiment, as mentioned above, a thin-type semiconductor package is realized by providing 5 a semiconductor chip C and projection electrodes T on the same surface side of a substrate 21 and resin-sealing them. Therefore, it is not necessary to pull leads outward of the package, so that the occupied area on the packaging 10 substrate 50 is reduced. Further, since the three-dimensional packaging or mounting of the semiconductor devices 20 is achieved by providing through holes 27 in the substrate 21, it is not necessary to individually bond leads of each layer of semiconductor device 20 to the packaging substrate, unlike the 15 aforementioned conventional art. Accordingly, the three-dimensional packaging of the semiconductor devices 20 can be extremely simply achieved.

Further, the projection electrodes T, being surrounded by the protective resin 25 (insulator), are 20 electrically stable without generating leak current or the like, and mechanically stable without being deformed or broken.

Further, by using the projection electrodes T, the wiring distance between the semiconductor chip C of an 25 upper semiconductor device and a lower semiconductor chip

C becomes short, and advantageously, highly speeding up of the electrical operation can be realized.

When specified projection electrodes T of a specified semiconductor device 20 of the plurality of vertically stacked semiconductor devices 20 are desired to be independently connected to the packaging substrate 50, the structure shown in Fig. 14 can be adopted. That is, on the substrates 21 of the lower semiconductor devices 20 than the specified semiconductor device 20, independent (i.e. electrically unconnected to the semiconductor chips C of the lower semiconductor devices 20 than the specified semiconductor device 20) junction projection electrodes Tc are provided at the positions corresponding to the specified projection electrodes T. Thereby, the specified projection electrodes T of the specified semiconductor device 20 can be connected through the junction projection electrodes Tc to the packaging substrate 50 independently of other semiconductor devices 20.

In the above-mentioned description of this embodiment, a plurality of semiconductor devices 20 having the same size semiconductor chips C respectively are stacked and three-dimensionally packaged. However, by aligning projection electrodes T as shown in fig.15, a plurality of semiconductor devices 100 containing different-sized semiconductor chips C respectively can be

three-dimensionally packaged similarly to the above-mentioned embodiment.

Further, in the abovementioned embodiment, the semiconductor devices 20, 100 are packaged or mounted 5 face-up on the packaging substrate 50 with the semiconductor chips C thereof in the upward position. However, the semiconductor devices 20, 100 may be packaged or mounted face-down on the packaging substrate 50 with the semiconductor chips C thereof opposed to the packaging 10 substrate 50.

Further, in the above-mentioned embodiment, the solder balls 28 are provided in the through holes 27 in the substrate 21. However, cream solders, instead of the solder balls 28, may be provided in the through holes 27 15 to be connected to the packaging substrate 50 or another layer of semiconductor device 20 by reflowing.

Further, in the above-mentioned embodiment, the protective resin 25, the projection electrodes T and the inactive surface C<sub>b</sub> of the semiconductor chip C are in the 20 same plane. However, the head portions of the projection electrodes T may be protruded from the upper surface of the protective resin 25, as in the eighth embodiment shown in Fig. 16. Further, the inactive surface C<sub>b</sub> side of the semiconductor chip C may be protruded from the upper 25 surface of the protective resin 25, as in the ninth

embodiment shown in Fig. 17. The structure shown in Figs. 16 or 17 can be fabricated by sufficiently thinning the protective resin 25. In this case, if the protective resin 25 tends to adhere to the head portions of the projection electrodes T, the protective resin adhered to the head portions of the projection electrodes T can be removed by polishing or grinding using a grinder or the like or etching.

Further, in the above-mentioned embodiment, one 10 semiconductor chip C is bonded onto the substrate 21 to fabricate the semiconductor device 20, 100. However, it is possible to bond two or more semiconductor chips C in common onto a substrate 21 so as to fabricate a semiconductor device 25 containing more than one 15 semiconductor chip C.

Further, in the above-mentioned embodiment, the projection electrodes T are cylindrical, but they may be in the form of bumps.

Further, in the above-mentioned embodiment, in the 20 manufacturing process, plurality of semiconductor chips C are resin-sealed as a whole, but every semiconductor chip C or every two or three (i.e. a predetermined plurality of) semiconductor chips C may be resin-sealed.

Further, in the above-mentioned each embodiment, 25 mechanical grinding using a grinder is performed in the

grinding step, but the grinding step may comprise a chemical grinding step using an etching liquid or a chemical and mechanical polishing step such as CMP (chemical and mechanical polishing) method. However,  
5 since the grinding speed is made more account of than the grinding precision in grinding or polishing the inactive surface side of the semiconductor chip C, the mechanical grinding method using a grinder is the most preferable among the above-mentioned three methods from a viewpoint  
10 of improving the manufacturing efficiency.

The resin and the inactive surface of the semiconductor chip mechanically ground by a grinder will have grinding traces thereon. However, such grinding traces can be cleaned at need by a chemical method such  
15 as etching or the like.

Further, in the above-mentioned embodiments, a dicing saw is used in the cutting out step for cutting out pieces of semiconductor devices. However, other cutting methods such as cutting with laser beam may be applied.

20 Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the  
25 terms of the appended claims.

This application corresponds to the Japanese Patent Applications No.11-235619 and No.11-235620 filed in the Japan Patent Office on August 23, 1999, No.11-257589 filed in the Japan Patent Office filed on September 10, 1999 and  
5 No. 11-292703 filed in the Japan Patent Office on October 14, 1999, the whole disclosures of these applications being incorporated herein by reference.

What is claimed is:

1. A method for manufacturing a semiconductor device,  
comprising:
  - an electrode forming step of forming projection  
electrodes on a surface of a semiconductor substrate,  
a step of forming a protective resin layer on a whole  
region of the surface of the semiconductor substrate  
provided with the projection electrodes,
  - a back side grinding step of thinning the  
semiconductor substrate by polishing or grinding a back  
side of the semiconductor substrate, and
  - a surface grinding step of exposing the projection  
electrodes by polishing or grinding the surface side of  
the semiconductor substrate.
- 15 2. A method for manufacturing a semiconductor device  
as claimed in claim 1, in which  
elements constituting a plurality of semiconductor  
devices are formed on the semiconductor substrate, and  
a plurality of groups of projection electrodes for  
20 the plurality of the semiconductor devices are formed  
in the electrode forming step,  
the method further comprising a cutting out step of  
cutting out pieces of semiconductor devices by cutting  
the semiconductor substrate after completing the surface  
25 grinding step and the back side grinding step.

3. A method for manufacturing a semiconductor device,  
comprising:

a step of forming a surface resin layer on a surface  
of a semiconductor substrate,

5 a step of forming a back side resin layer on a back  
side of the semiconductor substrate, and

10 a back side grinding step of thinning the  
semiconductor substrate by removing the back side resin  
layer, through polishing or grinding, from the  
semiconductor substrate provided with the surface resin  
layer and the back side resin layer, and by further  
polishing or grinding the back side of the semiconductor  
substrate from which the back side resin layer has been  
removed.

15 4. A method for manufacturing a semiconductor device  
as claimed in claim 3, further comprising

20 a cutting out step of cutting out pieces of  
semiconductor devices by cutting the semiconductor  
substrate along cutting lines after completing the back  
side grinding step.

5. A method for manufacturing a semiconductor device  
as claimed in claim 3 or 4, further comprising

25 a step of forming projection electrodes on the  
surface of the semiconductor substrate before forming  
the surface resin layer.

6. A method for manufacturing a semiconductor device  
as claimed in claim 5, in which

the surface resin layer is formed in such a manner  
that the projection electrodes are embedded in the  
5 surface resin layer.

7. A method for manufacturing a semiconductor device  
as claimed in claim 5 or 6, further comprising

a surface grinding step of exposing the projection  
electrodes from the surface resin layer by polishing  
10 or grinding the surface resin layer.

8. A method for manufacturing a semiconductor device  
as claimed in claim 7, in which the surface grinding step  
is performed before the back side grinding step.

9. A method for manufacturing a semiconductor device  
15 as claimed in any of claims 3 to 8, in which the surface  
resin layer and the back side resin layer are so formed  
as to have substantially the same thicknesses  
respectively.

10. A semiconductor device comprising

20 a solid device,

a semiconductor chip bonded onto a surface of the  
solid device,

projection electrodes for external connection  
formed on the surface of the solid device, and

25 a protective resin layer for sealing the surface

of the solid device with head portions of the projection electrodes thereon exposed.

11. A semiconductor device as claimed in claim 10, in which the solid device includes another semiconductor  
5 chip.

12. A semiconductor device as claimed in claim 10 or 11, in which the semiconductor chip is bonded face-down onto the solid device with an active surface of the semiconductor chip opposed to the solid device.

10 13. A semiconductor device as claimed in claim 10, in which the solid device includes a substrate.

14. A semiconductor device as claimed in claim 13, in which the semiconductor chip is bonded face-down onto the substrate with an active surface of the semiconductor  
15 chip opposed to the substrate.

15. A semiconductor device as claimed in claim 13 or 14, in which the substrate is provided with through holes enabling the electrical connection from a back side of the substrate to base portions of the projection  
20 electrodes.

16. A semiconductor device as claimed in claim 15, in which the through holes are provided right below the projection electrodes.

17. A method for manufacturing a semiconductor device,  
25 comprising:

a chip bonding step of bonding a plurality of semiconductor chips face-down onto a surface of a semiconductor substrate with active surfaces of the semiconductor chips opposed to the surface of the  
5 semiconductor substrate,

an electrode forming step of forming a plurality of projection electrodes on the surface of the semiconductor substrate,

10 a resin sealing step of sealing, with a protective resin, the semiconductor chip and the exposed surface of the semiconductor substrate after forming the projection electrodes in such a manner that head portions of the projection electrodes are exposed, and

15 a cutting out step of taking out individual pieces of chip-on-chip type semiconductor devices by cutting the semiconductor substrate along predetermined cutting lines.

18. A method for manufacturing a semiconductor device as claimed in claim 17, in which the resin sealing step  
20 includes an electrode exposing step of exposing the head portions of the projection electrodes by removing a surface layer section of the protective resin.

19. A method for manufacturing a semiconductor device as claimed in claim 18, in which the electrode exposing  
25 step includes a chip grinding step of simultaneously

polishing or grinding the protective resin and an inactive surface side of the semiconductor chip.

20. A method for manufacturing a semiconductor device as claimed in any of claims 17 to 19, in which a back 5 side of the semiconductor substrate or an inactive surface side of the semiconductor chip is polished or ground before the cutting out step.

21. A method for manufacturing a semiconductor device as claimed in any of claims 17 to 20, in which the 10 projection electrodes are formed to be higher than the active surface of the semiconductor chip and lower than an inactive surface of the semiconductor chip.

22. A method for manufacturing a semiconductor device, comprising:

15 a chip bonding step of bonding a semiconductor chip face-down onto a surface of a substrate with an active surface thereof opposed to the surface of the substrate,

20 an electrode forming step of forming projection electrodes on the surface of the substrate so as to be protruded from the surface of the substrate, and

25 a resin sealing step of sealing, with a protective resin, the semiconductor chip and the projection electrodes in such a manner that head portions of the projection electrodes are exposed.

23. A method for manufacturing a semiconductor device  
as claimed in claim 22, in which

a plurality of semiconductor chips are bonded  
onto the substrate in the chip bonding step, and

5 a plurality of groups of projection electrodes  
corresponding to the plurality of semiconductor chips  
are formed in the electrode forming step,

the method further comprising a cutting out step  
of taking out individual pieces of semiconductor devices  
10 by cutting the substrate along predetermined cutting  
lines.

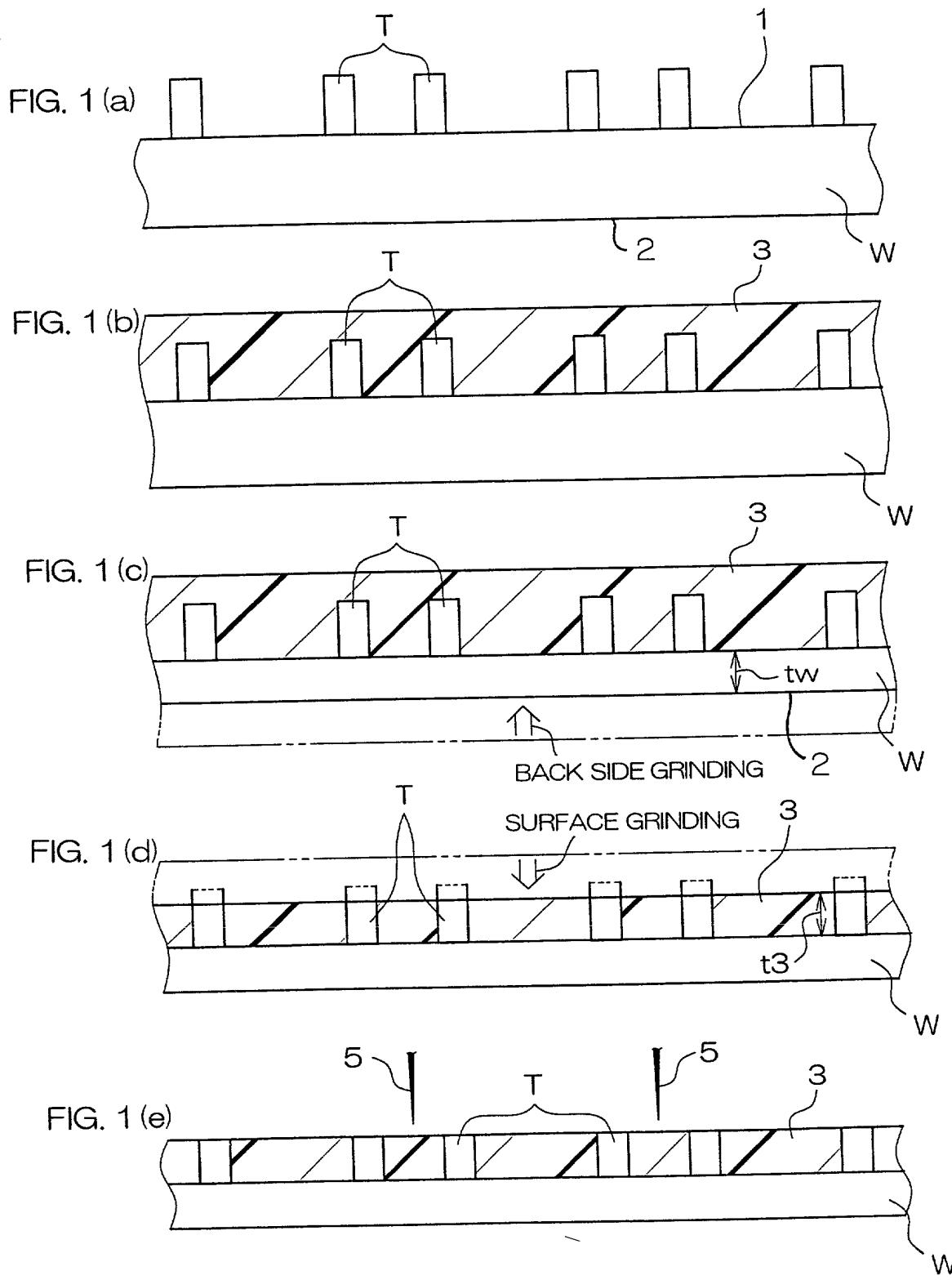
24. A method for manufacturing a semiconductor device  
as claimed in claim 22 or 23, further comprising a step  
of forming through holes enabling an electrical  
15 connection from a back side of the substrate to base  
portions of the projection electrodes.

25. A method for manufacturing a semiconductor device  
as claimed in any of claims 22 to 24, in which the resin  
sealing step includes a step of sealing, with a protective  
20 resin, the projection electrodes and the semiconductor  
chip and a step of removing a surface layer section of  
the protective resin so as to expose the head portions  
of the projection electrodes.

## ABSTRACT OF THE DISCLOSURE

A method for manufacturing a semiconductor device having projection electrodes on the surface of a semiconductor substrate. This method include an electrode forming step of forming the projection electrodes on the surface of the semiconductor substrate, a step of forming a protective resin layer on the whole surface of the semiconductor substrate provided with the projection electrodes, a back side grinding step of thinning the semiconductor substrate by polishing or grinding the back side of the semiconductor substrate, and a surface grinding step of exposing the projection electrodes by polishing or grinding the surface side of the semiconductor substrate.

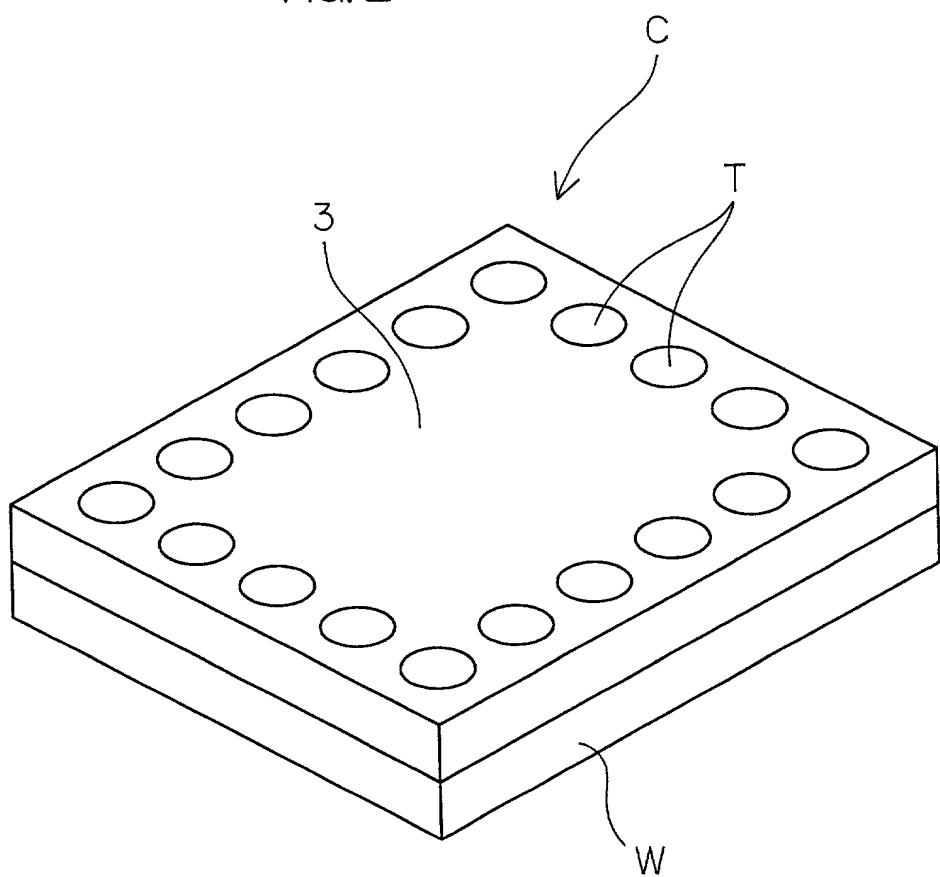
1/14



09/830092

2/14

FIG. 2



3/14

FIG. 3(a)

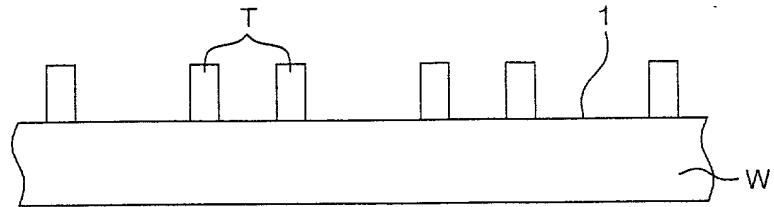


FIG. 3(b)

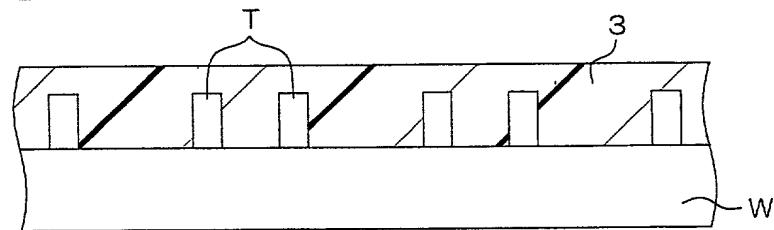


FIG. 3(c)

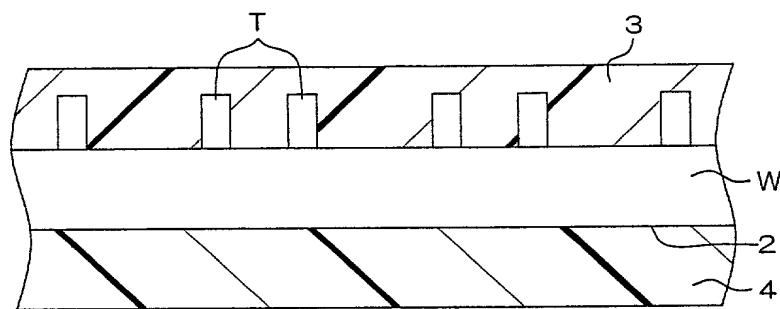


FIG. 3(d)

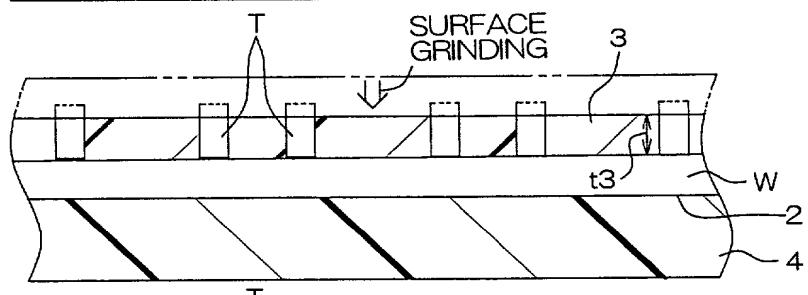


FIG. 3(e)

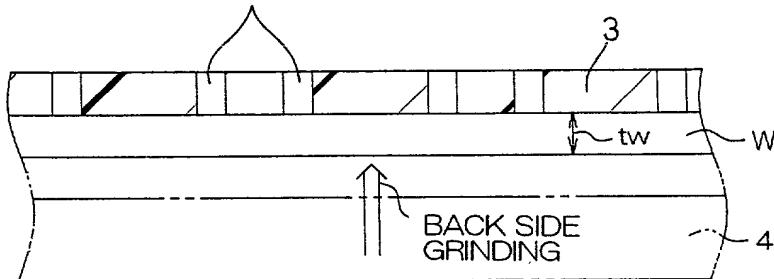
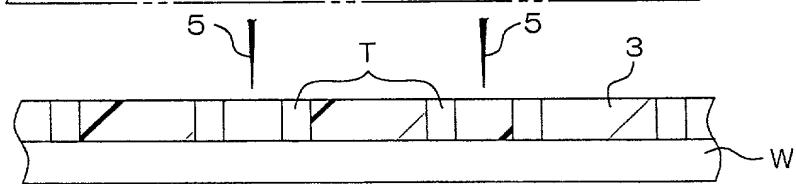


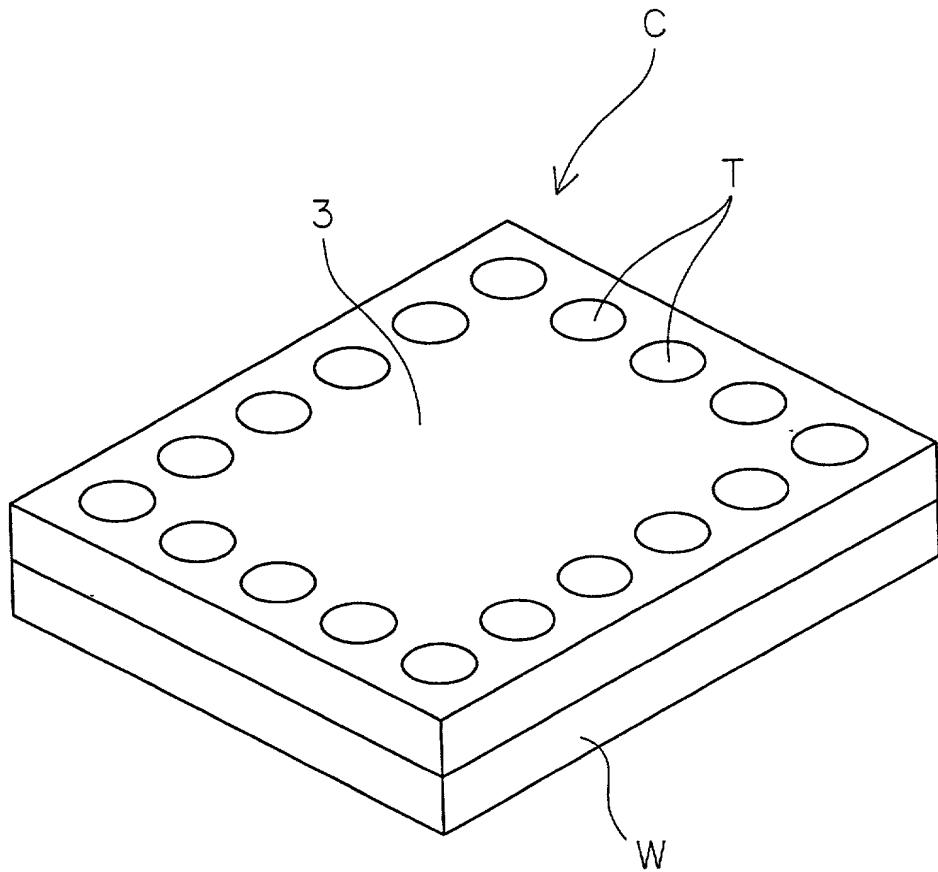
FIG. 3(f)



09/830092

4/14

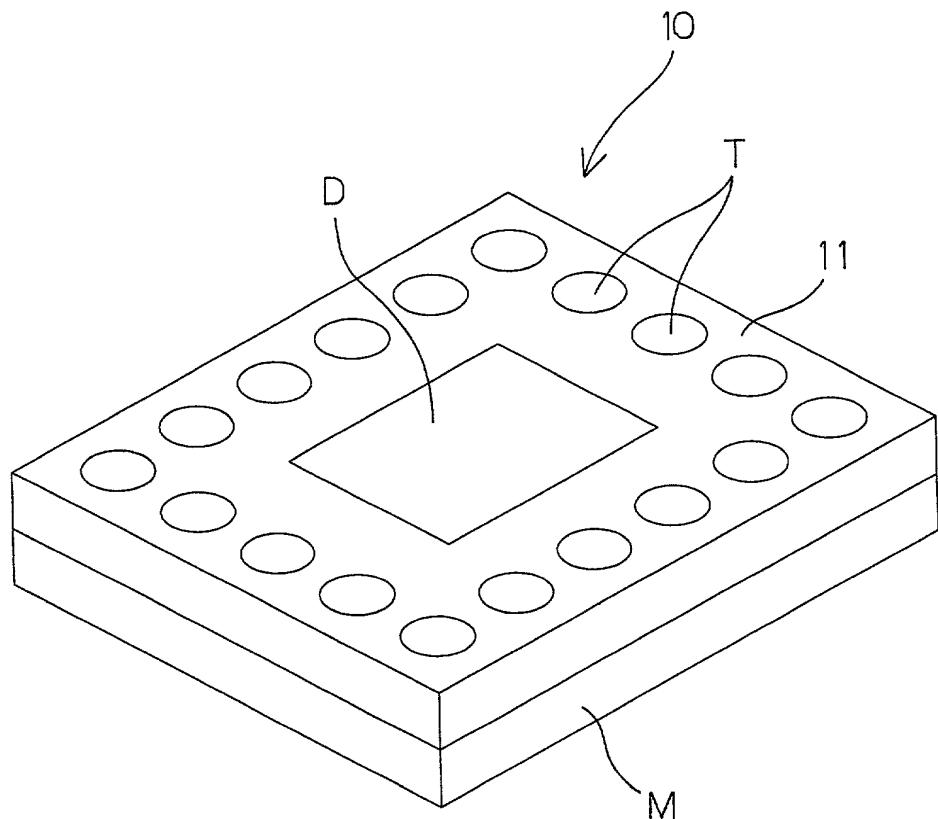
FIG. 4



09/830092

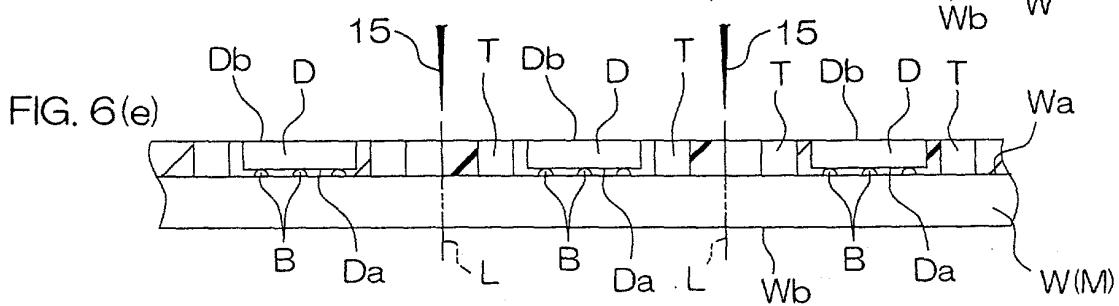
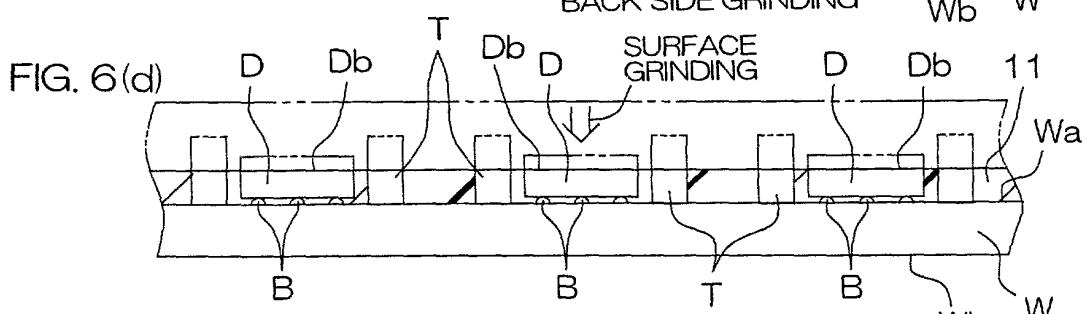
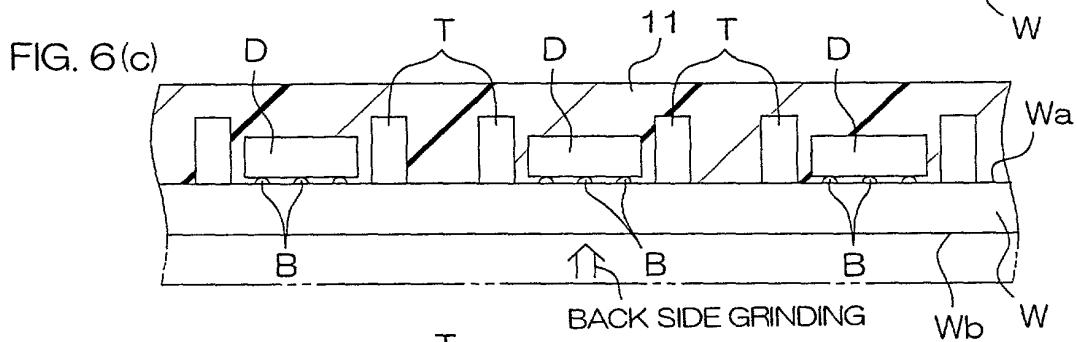
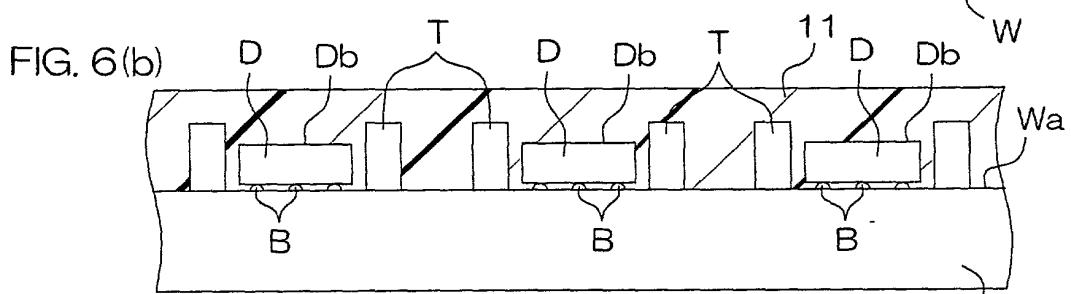
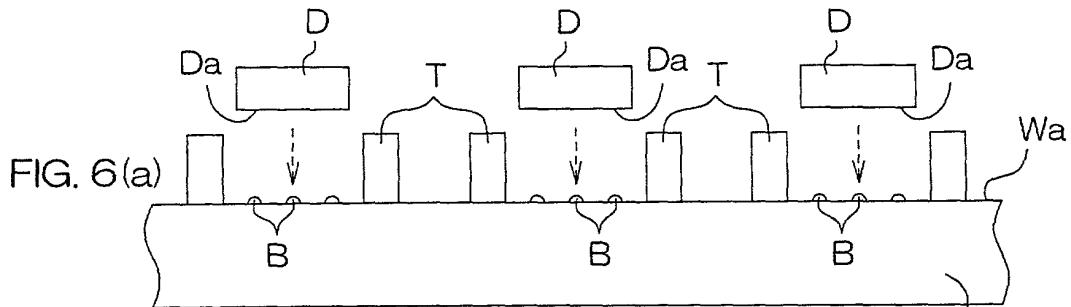
5/14

FIG. 5



09/830092

6/14



09/83092

7/14

FIG. 7

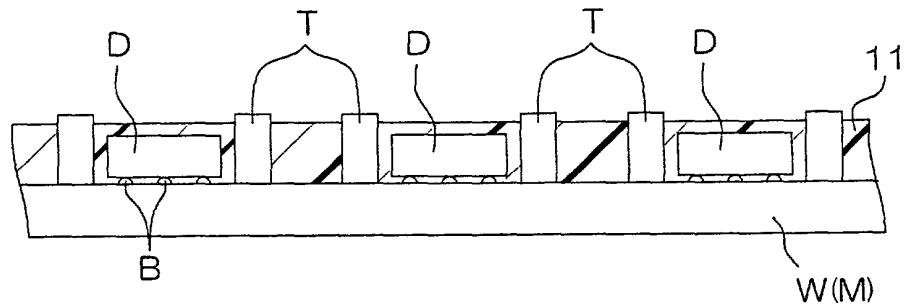


FIG. 8

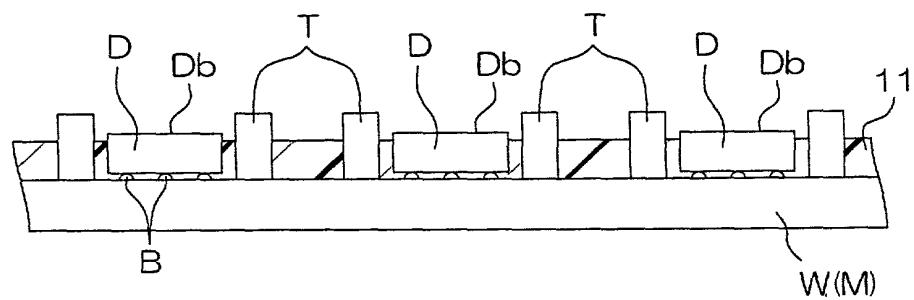
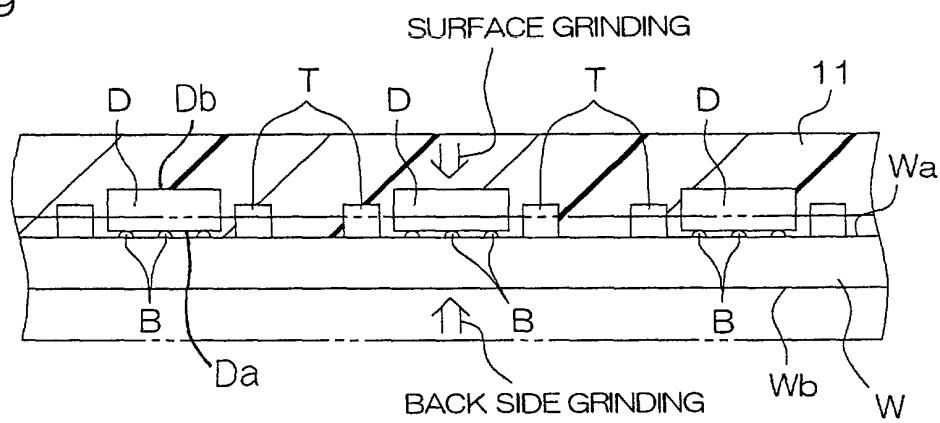
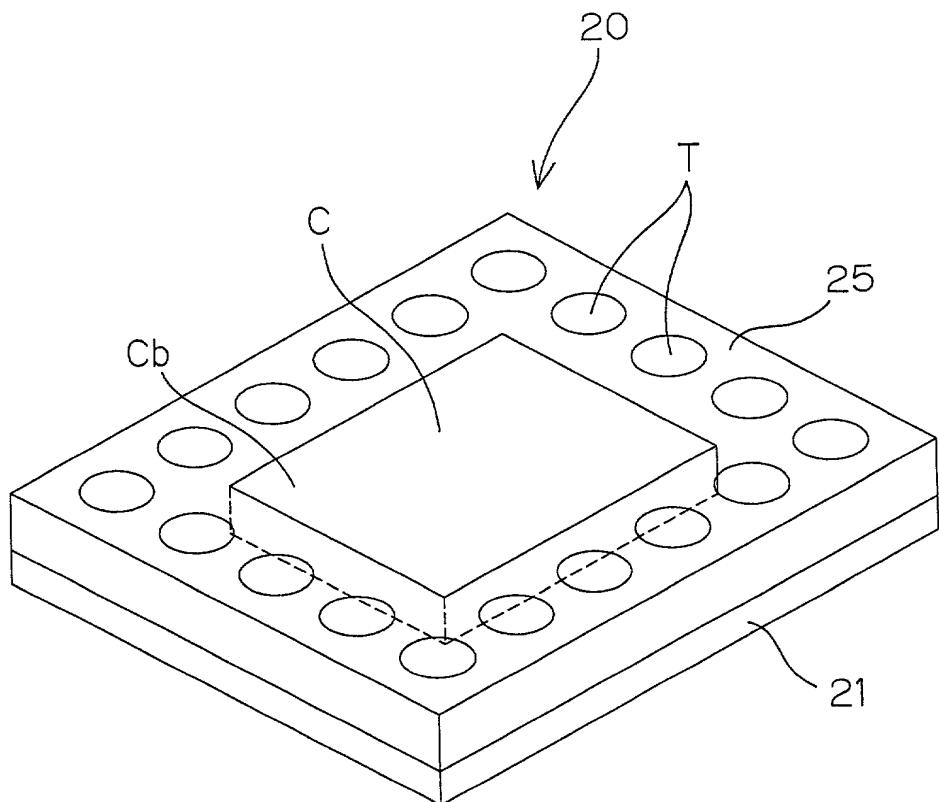


FIG. 9



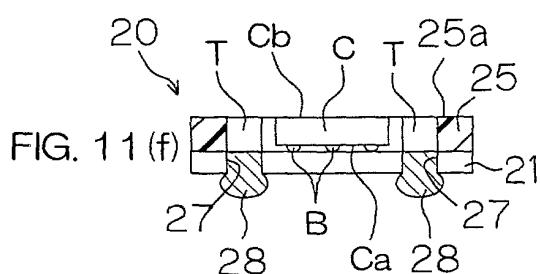
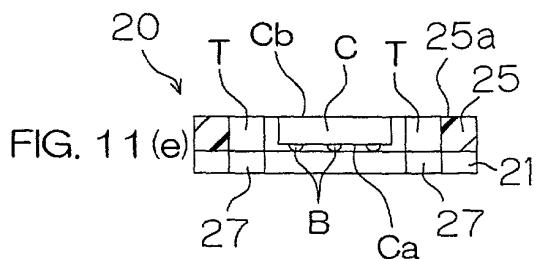
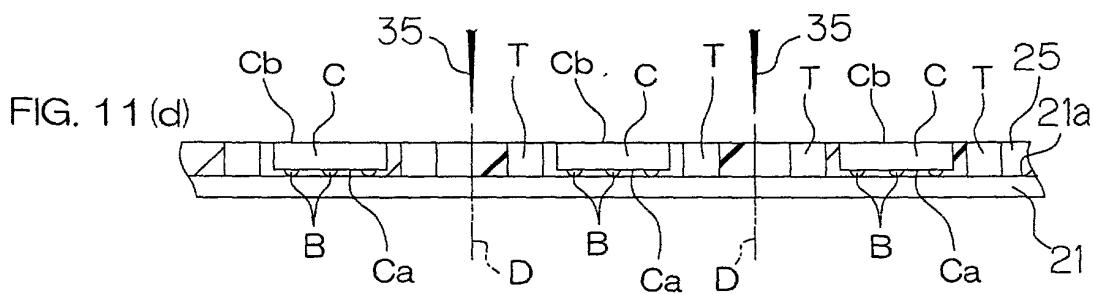
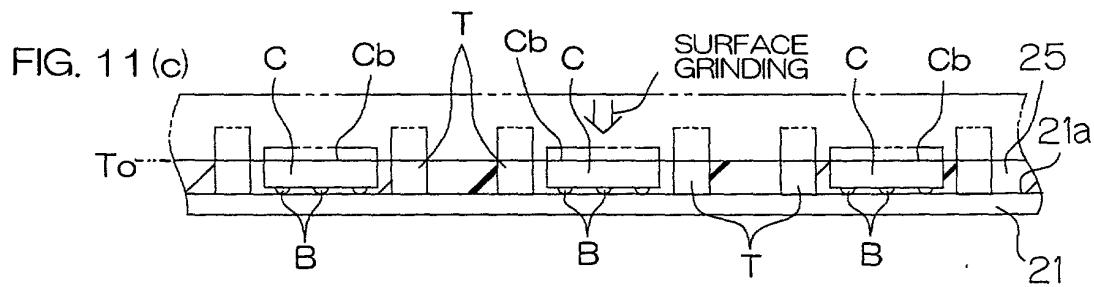
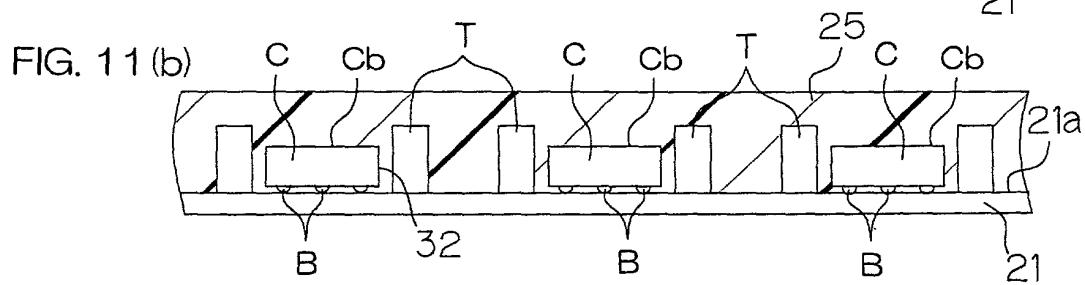
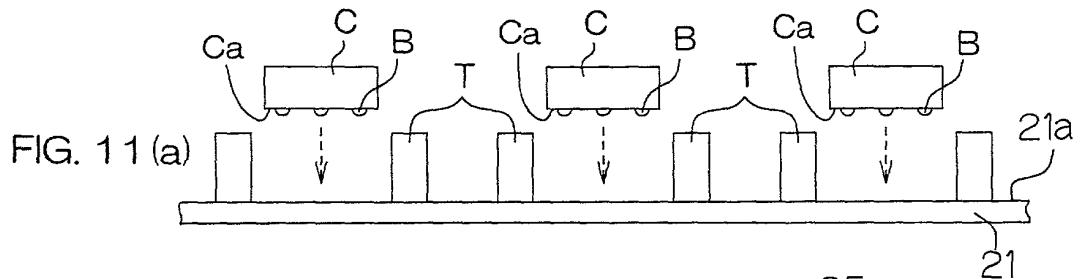
8/14

FIG. 10



09/830092

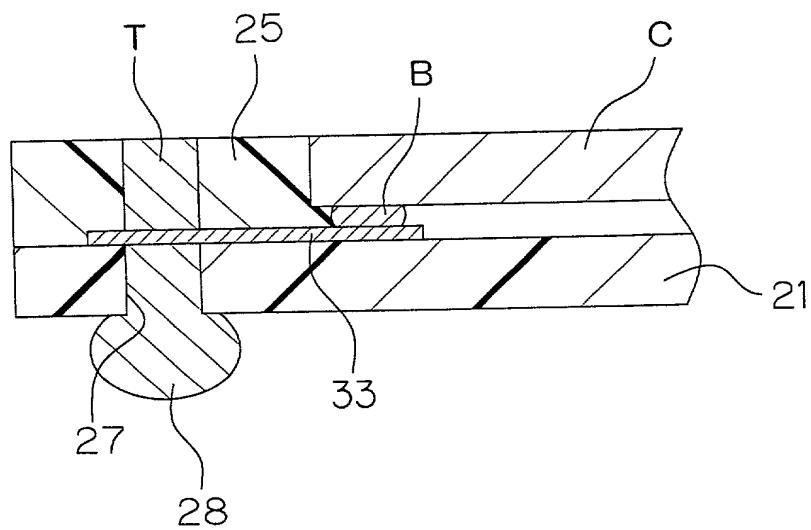
9/14



09/830092

10/14

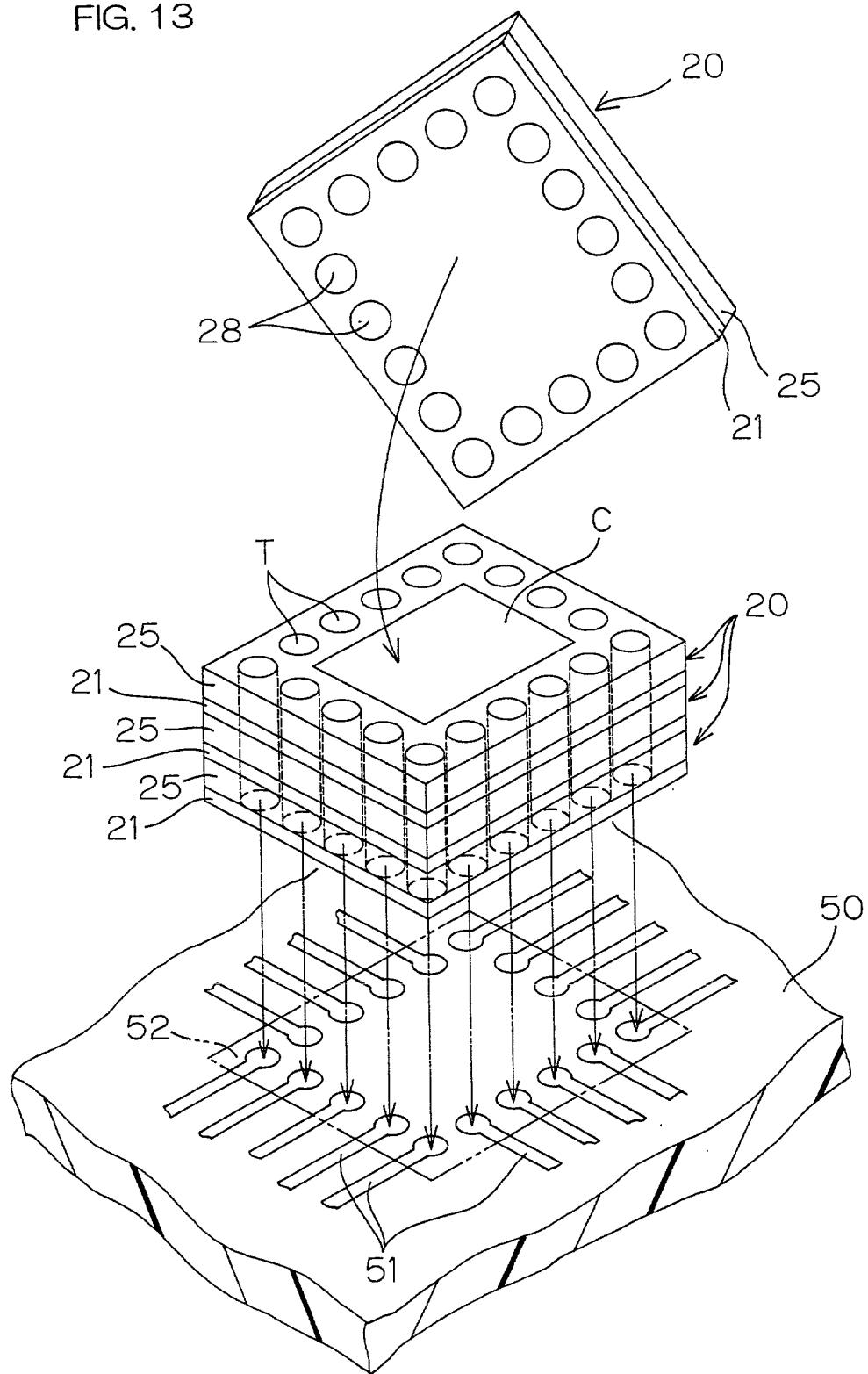
FIG. 12



09/830092

11/14

FIG. 13



09/830092

12/14

FIG. 14

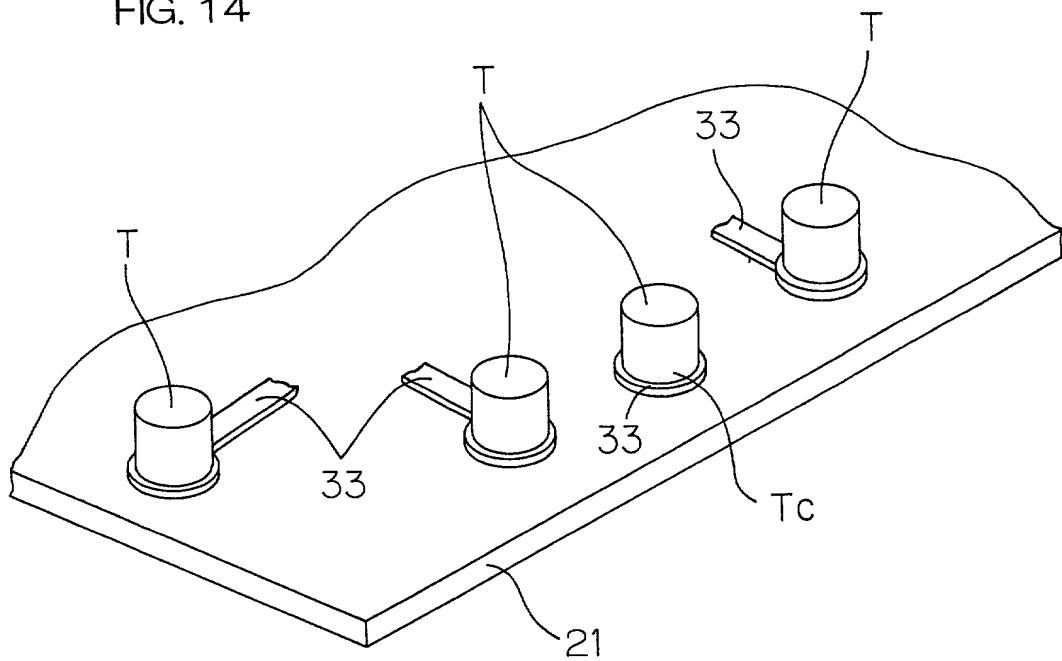
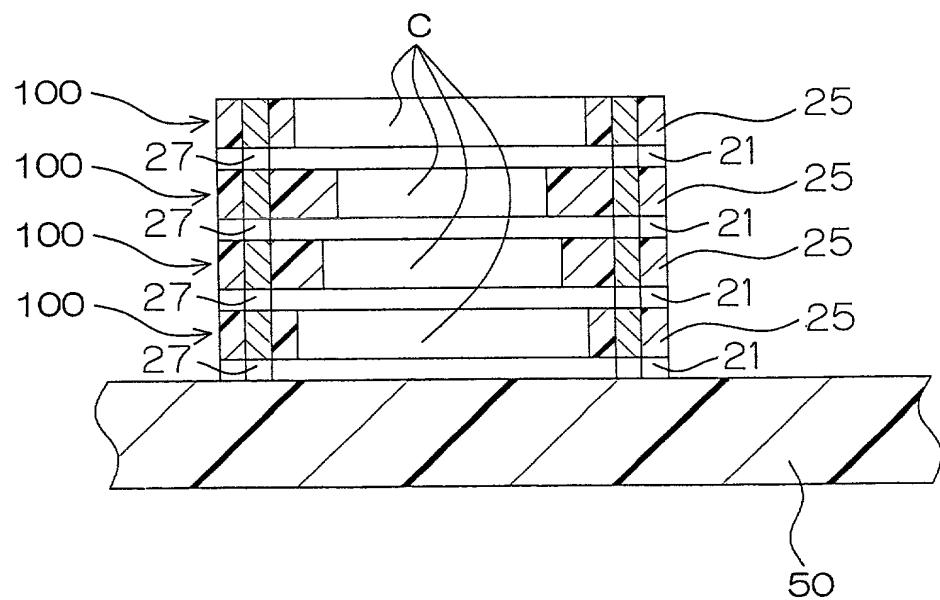


FIG. 15



09/830092

13/14

FIG. 16

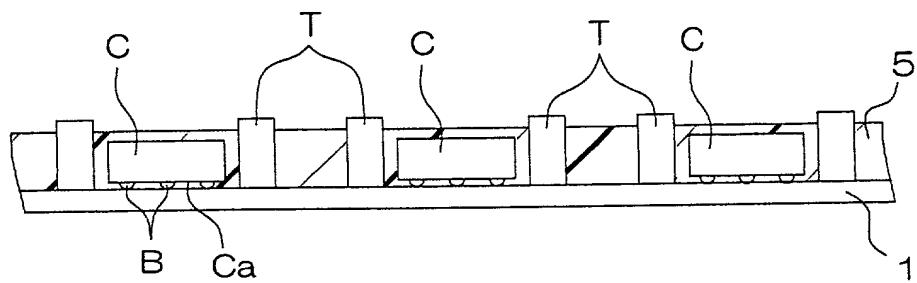


FIG. 17

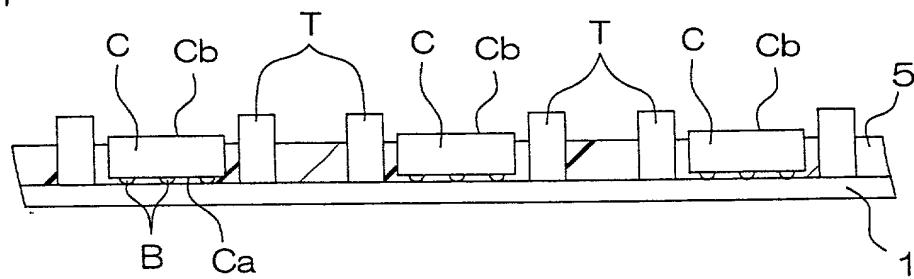
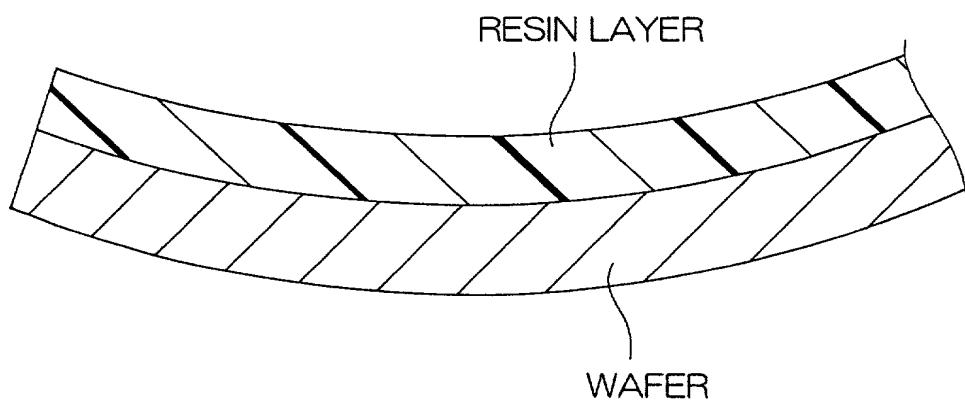


FIG. 18



09/830092

14/14

FIG. 19

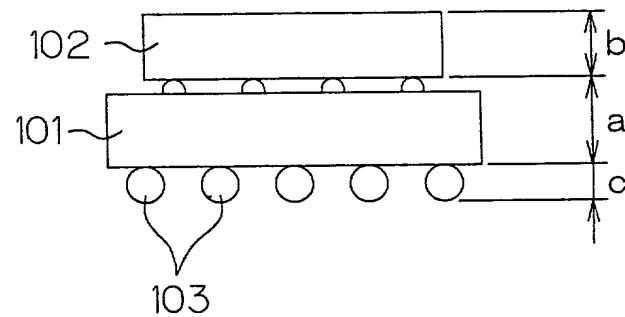
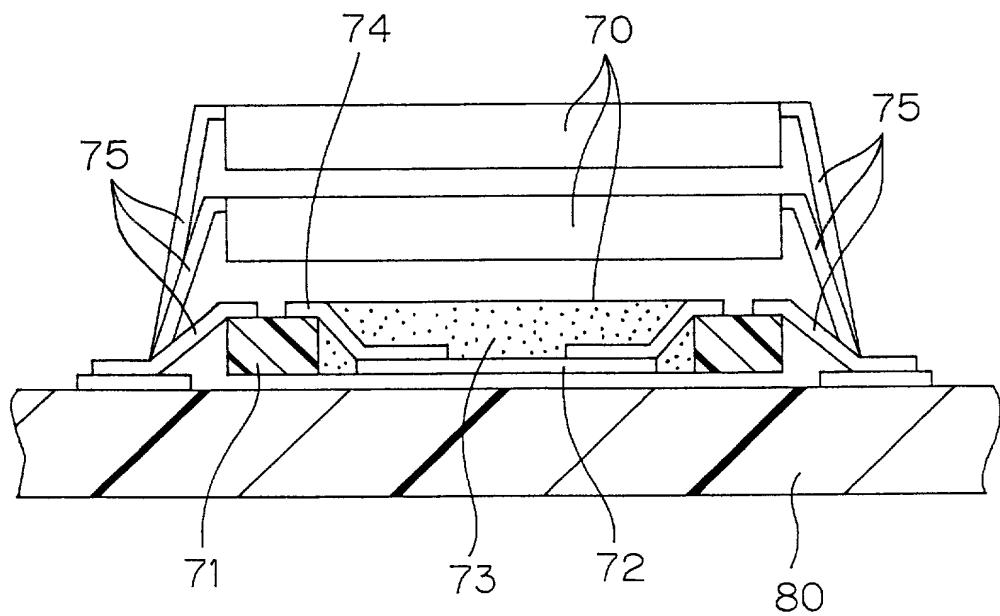


FIG. 20



Rec'd PCT/PTO 27 JUN 2001  
109/830092

ROH-037

PCT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the U.S. Nationalization Application of PCT/JP00/05596

Kazutaka SHIBATA

Group Unit:

Application No. 09/830,092

Examiner:

Filed: April 23, 2001

For: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING  
THE SAME

ASSOCIATE POWER OF ATTORNEY

Please recognize the following as having Associate Power of Attorney in this case:

Robert S. Green  
Registration No. 41,800

Brian K. Dutton  
Registration No. 47,255

and

Eugene G. Byrd  
Registration No. 47,361

of:

Rader, Fishman & Grauer PLLC  
1233 20<sup>th</sup> St., NW., Suite 501  
Washington, DC 20036

Please continue to direct all communication to the below address.

Respectfully submitted,

Ronald P. Mananen  
Reg. No. 24,104

DATE: June 27, 2001

**RADER, FISHMAN & GRAUER PLLC**

1233 20<sup>th</sup> Street, N.W. Suite 501

Washington, D.C. 20036

Tel: (202) 955-3750

Fax: (202) 955-3751

Customer No.: 23353

## Declaration and Power of Attorney For Patent Application

## 特許出願宣言書及び委任状

## Japanese Language Declaration

## 日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。 As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。 My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

---

SEMICONDUCTOR DEVICE AND METHOD FOR  
MANUFACTURING THE SAME

---

上記発明の明細書（下記の欄で x 印がついていない場合は、the specification of which is attached hereto unless the following 本書に添付）は、

\_\_\_\_月\_\_\_\_日に提出され、米国出願番号または特許協定条約  
国際出願番号を\_\_\_\_\_とし、  
(該当する場合) \_\_\_\_\_に訂正されました。

was filed on August 22, 2000  
as United States Application Number or  
PCT International Application Number  
PCT/JP00/05596 and was amended on  
\_\_\_\_\_ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

(Slight Modification was made at priority claiming portion.)

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

## Japanese Language Declaration (日本語宣言書)

私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基き下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約365(a)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願について外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

**Prior Foreign Application(s)**

外国での先行出願

**Priority Claimed**  
**優先権主張**

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Claimed 優先権主張
11-235619	Japan	23/08/1999	Yes
11-235620	Japan	23/08/1999	Yes
11-257589	Japan	10/09/1999	Yes
11-292703	Japan	14/10/1999	Yes

私は、第35編米国法典第119条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)
<p>私は、下記の米国法典第35編120条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約365条(c)に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。</p>			

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況: 特許許可済、係属中、放棄済)

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況: 特許許可済、係属中、放棄済)

私は、私自身の知識に基づいて本宣言書の中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣言を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

## Japanese Language Declaration (日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (*list name and registration number*).

Ronald P. Kananen	24,104	David L. Benson	42,314
John E. McGarry	22,360	Joel E. Bair	33,356
H. Lawrence Smith	24,900	Richard D. Grauer	22,388
Ralph T. Rader	28,772	Michael D. Fishman	31,951
Joseph V. Coppola, Sr.	33,373	Mark A. Davis	37,118
Michael B. Stewart	36,018	Stefan V. Chemielewski	39,914
Shmuel Livnat	33,949	Annette R. Carrothers	40,548
Steven L. Nichols	40,326	Kristin L. Murphy	41,212
Glenn E. Forbis	40,610	Christoper M. Tanner	41,518
Kevin D. Rutherford	40,412	Paul D. Amrozowicz	45,264
Alexander D. Rabinovich	37,425	G. Thomas Williams	42,228
Matthew J. Russo	41,282	John W. Rees	38,278
Monica Millner	42,894		

## 書類送付先

Monica Millner  
Rader, Fishman & Grauer PLLC  
1233 20<sup>th</sup> Street, N.W. Suite 501  
Washington, D.C. 20036

## Send Correspondence to:

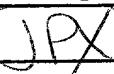
Monica Millner  
Rader, Fishman & Grauer PLLC  
1233 20<sup>th</sup> Street, N.W. Suite 501  
Washington, D.C. 20036

## 直接電話連絡先：（名前及び電話番号）

## Direct Telephone Calls to: (name and telephone number)

Telephone: (202) 955-3750  
Facsimile: (202) 955-3751

Telephone: (202) 955-3750  
Facsimile: (202) 955-3751

唯一または第一発明者名	Full name of sole or first inventor Kazutaka SHIBATA		
発明者の署名	日付	Inventor's signature 	Date April 27, 2001
住所	Residence Kyoto, Japan 		
国籍	Citizenship Japan		
私書箱	Post Office Address c/o ROHM CO., LTD., 21, Saiin Mizosaki-cho, Ukyo-ku, Kyoto 615-8585, Japan		
第二共同発明者	Full name of second joint inventor, if any		
第二共同発明者の署名	日付	Second inventor's signature	Date
住所	Residence		
国籍	Citizenship		
私書箱	Post Office Address		

(第三以降の共同発明者についても同様に記載し、署名をすること)  
(Supply similar information and signature for third and subsequent joint inventors.)